PMA15101 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- Acquire the fundamental knowledge of fuzzy sets,fuzzy logic,fuzzy decision making and fuzzy control systems.
- Learn about Matrix theory and Dynamic Programming.
- Expose the students to solve ordinary differential equations by various techniques. To know about Queuing Models.

UNIT I FUZZY LOGIC 9+6

Classical logic –Multi valued logics–Fuzzy propositions –Fuzzy quantifiers.

UNIT II MATRIX THEORY 9+6

Generalized Eigen values and Eigen vector–Some important matrix factorizations–The Cholesky decomposition–QR factorization–Least squares method–Singular valued composition-Toeplitz matrices and some applications.

UNIT III ONEDIMENSIONALRANDOMVARIABLES 9+6

Random variables - Probability function – moments – moment generating functions and their properties –Binomial ,Poisson ,Geometric, Uniform,Exponential,Gamma and Normal distributions.

UNIT IV DYNAMICPROGRAMMING 9+6

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming– Problem of dimensionality.

UNIT V QUEUINGMODELS 9+6

Markovian queues – Single and Multi-server Models – Little‟s formula -Machine Interference Model – SteadyStateanalysis– SelfService queue.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand the basic principles of fuzzy logic.
- Gain knowledge about Matrix theory and Dynamic Programming
- Develop difficiental algorithms for solving dynamic programming problems ,to acquire skills in handling situation involving random variable
- Analyze queuing models.

TEXT BOOKS

1. GeorgeJ.KlirandYuan,B.,“Fuzzysetsandfuzzylogic,Theoryandapplications”,PrenticeHallofIndia Pvt.Ltd., 1997.
2. Moon,T.K.,Sterling,W.C.,“Mathematicalmethodsandalgorithmsforsignalprocessing”,PearsonEducation,200.

3. RichardJohnson,Miller&Freund"ProbabilityandStatisticsforEngineers",7thEdition,PrenticeHallof India,Private Ltd., NewDelhi,2007.
4. TahaH.A.,"OperationsResearch-AnIntroduction",7thedition,Pearsoneducationeditions,Asia,New Delhi,2002.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	**Programme Outcomes(POs)**													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	3	-	-	-	-	3	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO3	3	3	-	-	-	3	-	-	-	-	3	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO5	3	3	-	-	-	3	-	-	-	-	3	3	3	3

PAE15102 ADVANCED DIGITAL SIGNAL PROCESSING 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- impart knowledge on Multi rate Signal Processing and FIR Filter design
- develop fundamental understanding on Power Spectrum Estimation
- Study about Linear Estimation and Prediction.
- Impart knowledge about Adaptive Filters and Wavelet Transform

UNIT I MULTIRATE SIGNAL PROCESSING AND MULTIRATE FIR FILTERDESIGN 9+6

Introduction to Decimation and Interpolation-Design of FIR filters for sampling rate conversion–Applications of Interpolation and decimation in signal processing –Filter bank implementation –Two channel filter banks-QMF filter banks–Perfect Reconstruction Filter banks–tree structured filter banks.

UNIT II POWER SPECTRALESTIMATION 9+6

Estimation of spectra from finite duration observations of a signal – The Periodogram - Use of DFT in Power spectral Estimation–Non-Parametric methods for Power spectrum Estimation–Bartlett Welch and Blackman–Turkey methods –Comparison of performance of Non – Parametric power spectrum Estimationmethods – Parametric Methods - Yule-Walker equations, solutions using Durbin‟s algorithm ,AR, MA,ARMA model based spectral estimation. Application: speech enhancement using power spectrum estimation.

UNIT III LINEARESTIMATIONANDPREDICTION 9+6

Forward and Backward linear prediction, Filtering - FIR Wiener filter- Filtering and linear prediction, non-causal and causal IIR Wiener filters, Discrete Kalman filter

UNIT IV ADAPTIVEFILTERS 9+6

Principles of adaptive filter – FIR adaptive filter – Newton‟s steepest descent algorithm – Derivation of first order adaptive filter–LMS adaptation algorithms–Adaptive noise cancellation ,Adaptive equalizer ,Adaptive echo cancellers

UNIT V WAVELETTRANSFORM 9+6

Short Time Fourier Transform, Continuous and discrete wavelet transform, Multire solution analysis, Application of wavelet transform, Cepstrum and Homomorphic filtering

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand Multirate Signal Processing
- Gain knowledge about Power Spectrum Estimation
- Explain the linear estimation and prediction

- Learn about Adaptive Filters
- Analyze the wavelet transforms.

TEXT BOOKS

1. Monson H,Hayes, "Statistical Digital Signal Processing and Modeling",JohnWiley and SonsInc.,New York,Indian Reprint,2007.
2. Rafae lC.Gonzalez, Richard E.Woods, "Digital Image Processing",Pearson,SecondEdition,2004.
3. (For Wavelet Transform Topic) JohnG.Proakis,Dimitris G. Manolakis,"Digital Signal Processing",Pearson,Fourth2007.
4. SophoclesJ.Orfanidis, "Optimum Signal Processing-AnIntroduction",McGrawHill,1990

Mapping of Course Outcomes with Programme Outcomes:

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COs	**Programme Outcomes(POs)**													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO2	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO3	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO4	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO5	3	3	3	3	-	-	-	-	-	-	-	3	3	3

PAE15103 ADVANCED DIGITAL LOGIC SYSTEM DESIGN 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- Familiarize the practical issues of sequential circuit design
- understand the concepts of Asynchronous Sequential Circuit Design.
- Study the concepts &gain knowledge about different fault diagnosis and testing methods
- study the performance estimation of digital systems.
- design & timing Analysis of memories

UNITI SEQUENTIAL CIRCUIT DESIGN 9+6

Analysis of Clocked Synchronous Sequential Networks (CSSN) - Modeling of CSSN – State Assignment and Reduction – Design of CSSN – Design of Iterative Circuits– ASM Chart – ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9+6

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Design of Hazard free circuits - Data Synchronizers –Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits. Practical issues such as clock skew, synchronous and asynchronous inputs and switch bouncing

UNIT III FAULT DIAGNOSIS AND TESTING 9+6

Fault diagnosis: Fault Table Method – Path Sensitization Method – Boolean Difference Method –Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm. Design for testability: Test Generation – Masking Cycle – DFT Schemes. Circuit testing fault model, specific and random faults, testing of sequential circuits, Built-in Self-Test, Built in Logic Block observer (BILBO), signature analysis.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9+6

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA– Xilinx 2000 -Xilinx 3000.

UNIT V SYSTEM DESIGN USING VHDL 9+6

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary

Divider – complete Sequential Systems – Design of a Simple Microprocessor

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Learn the synchronous sequential circuit design.
- Learn the design of Asynchronous sequential circuit design
- Know about Fault Diagnosis& Testing Methods
- Study the performance estimation of digital systems.
- Design timing Analysis of memories

REFERENCES

1. Charles H.Roth, "Fundamentals of Logic Design", Thomson Learning 2004.
2. ParagK.Lala "An introduction to Logic Circuit Testing", Morgan and claypool publishers, 2009.
3. J.F.Wakerly, "Digital Design principles and practices", PHI publications, 2005.
4. G.DonaldGivone, "Digital principles and Design", Tata McGraw Hill 2002.
5. H.Charles Roth, "Digital System Design using VHDL", Thomson Learning, 2007.

Mapping of Course Outcomes with Programme Outcomes:

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COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	3	-	-	2	-	-	-	3	3
CO2	3	3	-	-	-	-	-	-	2	-	-	-	3	3
CO3	3	3	-	-	-	3	-	-	2	-	-	-	3	3
CO4	3	3	-	-	-	-	-	-	2	-	-	-	3	3
CO5	3	3	-	-	-	3	-	-	2	-	-	-	3	3

PAE15104 ADVANCED MICROPROCESSOR AND MICRO-CONTROLLER 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- expose the students to the fundamentals of microprocessor architecture.
- introduce the advanced features in microprocessors and microcontrollers.
- enable the students to understand various microcontroller architectures
- understand in built function of PIC controller.
- understand about special purpose processors.

UNIT I MICROPROCESSOR ARCHITECTURE 9+6

Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – register file Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline Hazards- The software model – functional description – CPU pin descriptions – RISC concepts – RISC Properties – RISC Evaluation- RISC Versus CISC- Virtual 8086 model – Interrupt processing -Instruction types – Addressing modes – Processor flags – Instruction set

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE-PENTIUM 9+6

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point UNIT-Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set –addressing modes –Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE-ARM 9+6

Organization of CPU – Bus architecture –Memory management UNIT - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV PIC MICRO-CONTROLLER 9+6

Altera Cyclone Processor – Audio codec – Video codec design- Platforms-General Purpose processor- Digital Signal Processor – Embedded Processor- Media Processor – Video Signal Processor- Custom Hardware-CO-Processor

UNIT V EMCANTENNAANDANTENNAMEASUREMENTS 9+6

Concept of EMC measuring antenna; Tx and Rx antenna factors; Log periodic dipole, Bi-conical, Ridgeguide, Multi turn loop; Antenna measurement and instrumentation – Gain, Impedance and antenna factormeasurement; Antennatestrange Design.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Design and implement of advanced microprocessors

- Know about the high performance RISC and CISC architecture
- Perform PIC microcontroller programming
- Know about the various special purpose processors.

TEXT BOOKS

1. Gene .H.Miller, “Micro Computer Engineering”, Pearson Education, 2003.
2. Steve Furber, “ARM System –On –Chip architecture”, Addision Wesley, 2000.
3. John .B.Peatman, “Design with PIC Microcontroller”, Prentice hall, 1997.
4. .James L.Antonakos, “An Introduction to the Intel family of Microprocessors”, Pearson Education 1999.
5. Iain E.G.Richardson, “Video Codec Design”, John Wiley & Sons ltd, U.K, 2002.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	**Programme Outcomes(POs)**													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	-	3	3	3

PAE15105 MULTICORE ARCHITECTURE AND PROGRAMMING 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- introduce the recent trends in the field of Multicore processor.
- understand the challenges in parallel and multi-threaded programming.
- learn about the various parallel programming paradigms, and solutions.

UNIT I MULTI-CORE PROCESSORS 9+6

Single core to Multi-core architectures – SIMD and MIMD systems – Interconnection networks - Symmetric and Distributed Shared Memory Architectures – Cache coherence- Performance Issues – Parallel program design.

UNIT II PARALLEL PROGRAM CHALLENGES 9+6

Performance – Scalability – Synchronization and data sharing – Data races – Synchronization primitives (mutexes, locks, semaphores, barriers) – deadlocks and live locks – communication between threads (condition variables, signals, message queues and pipes)

UNIT III SHARED MEMORY PROGRAMMING WITH OPEN MP 9+6

Open MP Execution Model – Memory Model – Open MP Directives – Work-sharing Constructs – Library functions – Handling Data and Functional Parallelism – Handling Loops – Performance Considerations.

UNIT IV DISTRIBUTED MEMORY PROGRAMMING WITH MPI 9+6

MPI program execution – MPI constructs – libraries – MPI send and receive – Point-to-point and Collective communication – MPI derived data types – Performance evaluation

UNIT V PARALLEL PROGRAM DEVELOPMENT 9+6

Case studies - n-Body solvers – Tree Search – Open MP and MPI implementations and comparison.

TOTAL PERIODS 45+30

COURSE OUTCOMES

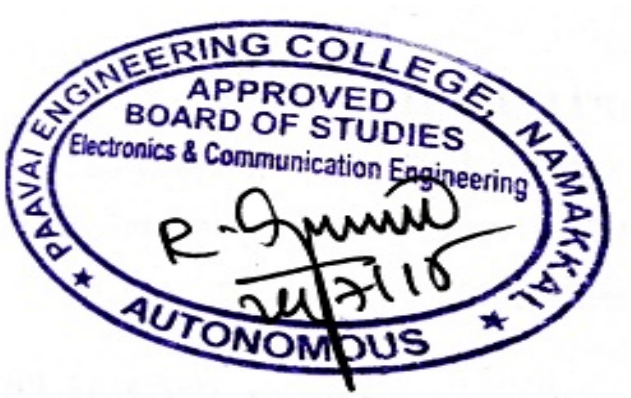
At the end of the course, the students will be able to

- Program Parallel Processors.
- Develop programs using Open MP and MPI.
- Compare and contrast programming for serial processors and programming for parallel processors.

TEXT BOOKS

1. Michael J Quinn, “Parallel programming in C with MPI and Open MP”, Tata McGraw Hill, 2003.
2. Peter S. Pacheco, “An Introduction to Parallel Programming”, Morgan Kauffman/Elsevier, 2011
3. Darryl Gove, “Multicore Application Programming for Windows, Linux, and Oracle Solaris”, Pearson, 2011
4. John L. Hennessey and David A. Patterson, “Computer Architecture – A Quantitative Approach”, Morgan Kaufmann / Elsevier, 5th edition, 2012
5. Kai Hwang, “Advanced Computer Architecture”, Tata McGraw-Hill Education, 2003.

Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**														
COs	**Programme Outcomes(POs)**													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	3	-	-		-	3	-	3	3
CO2	3	3	-	-	-	-	-	-		-	3	-	3	3
CO3	3	3	-	-	-	3	-	-		-	3	-	3	3
CO4	3	3	-	-	-	-	-	-		-	3	-	3	3
CO5	3	3	-	-	-	3	-	-		-	3	-	3	3



PAE15201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- impart knowledge on the CMOS Technology and Modeling of devices
- understand the basic concepts of CMOS operational amplifiers
- find the optimum solution of the complex problem in multistage amplifier.
- Acquire the knowledge of biasing circuit, stability and frequency compensation

UNIT I CMOS TECHNOLOGY AND DEVICE MODELING 9+6

Basic MOS semiconductor fabrication processes-other considerations of CMOS technology-MOS large signal model and parameters-Small signal model for the MOS transistor-Computer simulation models-Sub threshold MOS model.

UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS 9+6

Miller effect, Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise -noise in single stage amplifiers, noise in differential amplifiers.

UNIT III CMOS OPERATIONAL AMPLIFIERS 9+6

Buffered operational amplifiers-High speed and frequency operational amplifiers-Differential output operational amplifiers-Microwave operational amplifiers - Low noise operational amplifiers - Low voltage operational amplifiers.

UNIT IV STABILITY AND FREQUENCY COMPENSATION 9+6

General considerations, Multipole systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, and Other compensation techniques.

UNIT V BIASING CIRCUITS 9+6

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm biasing.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Explain CMOS technology and device modeling
- Perform analysis on frequency response
- Explain about CMOS operational amplifiers, stability and frequency compensation
- Know about Biasing circuits

REFERENCES

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition, Wiley, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.
3. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
5. Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002 ..

Mapping of Course Outcomes with Programme Outcomes:

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COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	3	-	-	-	-	3	3	-	3
CO2	3	3	-	-	-	-	-	-	-	-	3	3	-	3
CO3	3	3	-	-	-	3	-	-	-	-	3	3	-	3
CO4	3	3	-	-	-	-	-	-	-	-	3	3	-	3
CO5	3	3	-	-	-	3	-	-	-	-	3	3	-	3

PAE15202 **ASIC AND FPGA DESIGN** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- learn the fundamentals of ASIC and its design methods and the physical design of ASIC.
- learn logic synthesis and testing.
- gain knowledge on programmable architectures for ASICs
- learn concepts of system on chip design

UNIT I OVERVIEW OF ASIC AND PLA **9+6**

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Anti fuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II ASIC PHYSICAL DESIGN PROGRAMMABLE ASIC **9+6**

Systempartition-partitioning-partitioningmethods–interconnectdelaymodelsandmeasurementofdelay –floor planning- placement– Routing:globalrouting-detailedrouting-specialrouting–circuitextraction– DRC. Anti fuse - Static RAM - EPROM and EEPROM technology – Practical issues - PREP benchmarks -Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX – Xilinx Spartan – Virtex FPGAs – Altera CycloneFPGAs

UNIT III LOGIC SYNTHESIS AND SIMULATION TESTING **9+6**

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language -PLA tools - EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis -types of simulation - boundary scan test - fault simulation - automatic test pattern generation

UNIT IV FPGA ARCHITECTURE **9+6**

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology – mapping for FPGAs, Xilinx XC4000 - ALTERA‟s FLEX 8000/10000, ACTEL‟s ACT-1,2,3 and their speed performance Case studies: Altera MAX 5000 and 7000 - Altera MAX 9000 – Spartan II and Virtex II FPGAs – Apex and Cyclone FPGAs

UNIT V SOC DESIGN **9+6**

Design Methodologies – Processes and Flows - Embedded software development for SOC –Techniques for SOC Testing – Configurable SOC – Hardware / Software co-design Case studies: Digital camera, Bluetooth radio / modem, SDRAM and USB.

TOTAL PERIODS **45+30**

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand different types of ASIC‟s and physical design of ASIC.
- Understand logic synthesis and testing methods and different FPGA architectures.
- Design real time applications on SOC.

REFERENCES

1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc., 1997
2. R. Rajsuman, "System-on-a-Chip Design and Test", Santa Clara, CA: Artech House Publishers, 2000.
3. S.Trimberger, "Field Programmable Gate Array Technology", Edr, Kluwer Academic Publications, 1994..
4. John V.Oldfield, Richard C Dore, "Field Programmable Gate Arrays", Wiley Publications1995
5. P.K.Chan& S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall, 1994.

Mapping of Course Outcomes with Programme Outcomes:

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COs	**Programme Outcomes(POs)**													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	3	-	-	-	-	3		3	3
CO2	3	3	-	-	-	-	-	-	-	-	3		3	3
CO3	3	3	-	-	-	3	-	-	-	-	3		3	3
CO4	3	3	-	-	-	-	-	-	-	-	3		3	3
CO5	3	3	-	-	-	3	-	-	-	-	3		3	3

PAE15203 **LOW POWER VLSI DESIGN** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- know the sources of power consumption in CMOS circuits
- understand the various power reduction techniques and the power estimation methods
- study the design concepts of low power circuits

UNIT I POWER DISSIPATION IN CMOS **9+6**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

UNIT II POWER OPTIMIZATION **9+6**

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers - CMOS Circuits design styles, Adders, Multipliers

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS **9+6**

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV POWER ESTIMATION **9+6**

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis- Random Logic signals – Probabilistic power analysis techniques

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9+6**

4G features and challenges, Technology path, IMS Architecture, Convergent Devices, 4G technologies,AdvancedBroadbandWirelessAccessand Services,Multimedia,MVNO.

TOTAL PERIODS **45+30**

COURSE OUTCOMES

At the end of the course, the students will be able to

- Learn the basic concepts and principles of CMOS.
- Learn the techniques of reducing power consumption
- Know about advanced and special techniques for low power systems
- Learn about the techniques involved in power estimation
- Know about software design for Low Power.

REFERENCES

1. K.Roy and S.C. Prasad, “Low Power CMOS VLSI circuit design”, Wiley, 2000
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Circuits For Low Power”, Kluwer, 2002
3. J.B. Kuo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
4. Gary. S. Rogers & JohnEdwards, “An IntroductiontoWirelessTechnology”,Pearson Education,2007..
5. James B. Kuo, Shin – chia Lin, “Low voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and sons, Inc 2001.

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(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-		3	3	3
CO2	3	3	-	-	-	-	-	-	-	-		3	3	3
CO3	3	3	-	-	-	-	-	-	-	-		3	3	3
CO4	3	3	-	-	-	-	-	-	-	-		3	3	3
CO5	3	3	-	-	-	-	-	-	-	-		3	3	3

PAE15151 **ADVANCED DIGITAL IMAGE PROCESSING** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- introduce the basics of digital image processing.
- learn applications of segmentation with texture analysis
- introduce theory of Feature extraction
- cquire the concept of image fusion
- To study the applications of image processing

UNIT I FUNDAMENTALS OF DIGITAL IMAGE PROCESSING **9+6**

Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency domain, Review of morphological image processing

UNIT II SEGMENTATION AND TEXTURE ANALYSIS **9+6**

Edge Linking and Boundary Detection - Local Processing-Global Processing –Thresholding- Segmentation by Morphological Watershed Segmentation Algorithm - Use of Markers- Use of Motion in Segmentation- Spatial Techniques-Frequency Domain Techniques-Texture- Statistical, Syntactic and Hybrid texture description - texture recognition and applications

UNIT III FEATURE EXTRACTION **9+6**

First and second order edge detection operators, Phase congruency, Localized feature extraction detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Run length features, Fractal model based features, Gabor filter, wavelet features

UNIT IV REGISTRATION AND IMAGE FUSION **9+6**

Registration- Preprocessing, Feature selection-points, lines, regions and templates Feature correspondence- Point pattern matching, Line matching, and region matching Template matching. Transformation functions- Similarity transformation and Affine Transformation - Resampling- Nearest Neighbor and Cubic Splines Image Fusion-Overview of image fusion, pixel fusion, Multiresolution based fusion discrete wavelet transform, Curvelet transform - Region based fusion.

UNIT V IMAGE PROCESSING APPLICATIONS **9+6**

Image compression- JPEG, JPEG2000 and MPEG standards- Watermarking-Steganography-3D vision tasks-

Marr‟s theory, active and purposive vision- Geometry for 3D vision-Use of 3D vision-Shape from X-shape - motion, texture- Full 3D objects.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Learn the Basic Concepts of image processing
- Understand the working and applications of segmentation.
- Learn about 3D image visualization and image processing applications
- Know about working of image fusion

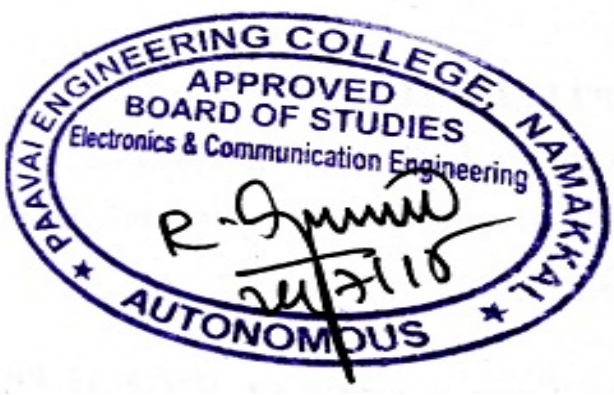
REFERENCES

1. John C.Russ, “The Image Processing Handbook”, CRC Press, 2007.
2. Mark Nixon, Alberto Aguado, “Feature Extraction and Image Processing”, Academic Press, 2008..
3. ArdeshirGoshtasby, “2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications”, John Wiley and Sons, 2005
4. H.B.Mitchell, “Image Fusion Theories, Techniques and Applications”, Springer, 2010.
5. Rafael C. Gonzalez, Richard E. Woods, “Digital Image Processing”, Pearson, Education, Inc., Second Edition, 2004.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	3	-	-	-	-		3	3	3
CO2	3	3	-	-	-	-	-	-	-	-		3	3	3
CO3	3	3	-	-	-	3	-	-	-	-		3	3	3
CO4	3	3	-	-	-	-	-	-	-	-		3	3	3
CO5	3	3	-	-	-	3	-	-	-	-		3	3	3



PAE15152 WAVELET TRANSFORMS AND APPLICATIONS 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- understand the fundamentals of Vector Analysis
- learn the concepts of multi resolution analysis.
- study the properties of continuous wavelet transforms.
- characterize Filter Bank and Sub Band Coding Principles
- study the various Image Compression Techniques.

UNIT I MATHEMATICAL FUNDAMENTALS 9+6

Linear spaces – Vectors and vector spaces – Basis functions – Dimensions –Orthogonality and bio-rthogonalilty– Local basis and Riesz basis – Discrete linear normed space – Approximation by orthogonal projection –Matrix algebra and linear transformation

UNIT II MULTI RESOLUTION ANALYSIS 9+6

DefinitionofMultiResolutionAnalysis(MRA)–HaarBasis–ConstructionofGeneralOrthonormalMRA

/avelet Basis for MRA – Continuous Time MRA Interpretation for the DTWT – Discrete Time MRA Basis Functions for the DTWT– PRQMF Filter Banks.

UNIT III CONTINUOUS WAVELET TRANSFORMS 9+6

Wavelet Transform – Definition and Properties – Concept of Scale and its Relation with Frequency – Continuous Wavelet Transform (CWT) – Scaling Function and Wavelet Functions (Daubechies Coiflet, Mexican Hat, Sinc, Gaussian, Bi Orthogonal) – Tiling of Time – Scale Plane for CWT.

UNIT IV DISCRETE WAVELET TRANSFORMS 9+6

Filter Bank and Sub Band Coding Principles – Wavelet Filters – Inverse DWT Computation by Filter Banks

– Basic Properties of Filter Coefficients – Choice of Wavelet Function Coefficients – Derivations of Daubechies Wavelets – Mallat's Algorithm for DWT – Multi Band Wavelet Transforms Lifting Scheme- Wavelet Transform Using Poly phase Matrix Factorization –Geometrical Foundations of Lifting Scheme – Lifting Scheme in Z – Domain.

UNIT V TRANSFORMS AND ITS APPLICATIONS 9+6

Wavelet methods for signal processing- Image Compression Techniques: EZW–SPHIT Coding –Image Denoising Techniques: Noise Estimation – Shrinkage Rules – Shrinkage Functions – Edge Detection and Object Isolation, Image Fusion, and Object Detection.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Apply the fundamentals of Vector Analysis.
- Know the concepts of multi resolution analysis..
- Understand the properties of continuous wavelet transforms
- Apply the knowledge of Filter Bank and Sub Band Coding Principles.
- Understand the various Image Compression Techniques.

REFERENCES

1. Rao R.M and A.S.Bopardikar, “Wavelet Transforms Introduction to theory and Applications”, Pearson Education, Asia, 2000
2. J.C.Goswami and A. K. Chan, “Fundamentals of wavelets: Theory, Algorithms and Applications", Wiley Inter science Publication, John Wiley & Sons Inc., 1999.
3. M.Vetterli, J.Kovacevic, “Wavelets and sub band coding", Prentice Hall Inc, 1995..
4. Stephen G. Mallat, “A wavelet tour of signal processing", 2nd Edition Academic Press, 2000.
5. Soman K.P and Ramachandran K.I, “Insight into Wavelets from Theory to practice”, Prentice Hall, 2004.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	-	3	3	3

PAE15153 **SOFT COMPUTING** **3 0 0 3**

COURSE OBJECTIVES

To enable the students to

- study different types of optimization techniques
- study genetic algorithms
- gain knowledge in neural networks
- study and analyze fuzzy logic
- understand the Neuro fuzzy modeling

UNIT I EVOLUTION OF COMPUTING **9**

Evolution of Computing - Soft Computing Constituents – From Conventional AI to Computational Intelligence - Machine Learning Basics

UNIT II GENETIC ALGORITHMS **10**

Introduction, Building block hypothesis, working principle, Basic operators and Terminologies like individual, gene, encoding, fitness function and reproduction, Genetic modeling: Significance of Genetic operators, Inheritance operator, cross over, inversion & deletion, mutation operator, Bitwise operator, GA optimization problems, JSPP (Job Shop Scheduling Problem), TSP (Travelling Salesman Problem),Differences & similarities between GA & other traditional methods, Applications of GA.

UNIT III NEURAL NETWORKS **9**

Machine Learning using Neural Network, Adaptive Networks – Feed Forward Networks– Supervised Learning Neural Networks – Radial Basis Function Networks - Reinforcement Learning– Unsupervised Learning Neural Networks – Adaptive Resonance Architectures – Advances in Neural Networks

UNIT IV FUZZY LOGIC AND SIMULATED ANNEALING **8**

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making, Annealing, Boltzmann machine – learning – application – Counter Propagation Network – architecture – training - Applications

UNIT V ADVANCED NEURO-FUZZY MODELING **9**

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control -Case Studies.

TOTAL PERIODS **45**

COURSE OUTCOMES

At the end of the course, the students will be able to

- Have insight into the fundamentals of soft computing
- Understand the genetic algorithm
- Design the neural network
- Perform advanced Neuro-Fuzzy Modeling

REFERENCES

1. Jyh-Shing Roger Jang, Chuen-Tsai Sun, EijiMizutani, "Neuro-Fuzzy and Soft Computing", Prentice-Hall of India, 2003.
2. S.Rajasekaran and G.A.VijayalakshmiPai, **"**Neural networks, Fuzzy logics and Genetic algorithms"**,** Prentice Hall of India, 2003.
3. KwangH.Lee, "First course on Fuzzy Theory and Applications", Springer–Verlag Berlin Heidelberg, 2005.
4. James A. Freeman and David M.Skapura, "Neural networks algorithms, applications, and programming techniques", Pearson edition, 2003.
5. David E.Goldberg, "Genetic Algorithms in Search, Optimization, and Machine Learning", Pearson Education, Asia, 2001.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	**Programme Outcomes(POs)**													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	3	3	3	3

PAE15154 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING 3 0 0 3

COURSE OBJECTIVES

To enable the students to

- know the basics of computer design and performance measures
- introduce the concepts parallel processing and pipelining
- educate about hardware technologies
- gain knowledge about multiprocessors
- introduce Multicore architectures

UNIT I THEORY OF PARALLELISM 9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multi vector and SIMD architectures – Multithreaded architectures – Data-flow architectures - Performance Measures

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III HARDWARE TECHNOLOGIES 9

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology- Bus cache and Shared Memory - backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models, Pipelining and superscalar Techniques.

UNIT IV MULTIPROCESSORS 9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES 9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies –Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture - hp architecture.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of the course, the students will be able to

- Learn the computer design Concepts
- Understand the parallel processing and pipelining
- Gain knowledge in memory hierarchy design
- Learn about multiprocessors and the multi-core architecture

REFERENCES

- Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.
- John L. Hennessey and David A. Patterson, “Computer Architecture – A quantitative approach”, Morgan Kaufmann / Elsevier, 4th. Edition, 2007.
- William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Seventh Edition, 2006.
- John P. Hayes, “Computer Architecture and Organization”, McGraw Hill
- David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A hardware/ software approach”, Morgan Kaufmann / Elsevier, 1997.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	-	3	3	3

PAE15251 **CAD FOR VLSI CIRCUITS** **3 0 0 3**

COURSE OBJECTIVES

To enable the students to

- introduce the basic CAD algorithm and Partitioning
- educate about Placement, Floor Planning
- learn about Global, Detail routing
- know the Modeling and synthesis in CAD flow.

UNIT I LOGIC SYNTHESIS& BASIC CAD ALGORITHMS 9

Introduction to combinational logic synthesis - Binary Decision Diagram - Hardware models for High-level synthesis - graph algorithms - computational geometry algorithms.

UNIT II PARTITIONING 9

Classification of partitioning algorithms - Group migration algorithms - simulated annealing & evolution, other partitioning algorithms

UNIT III PLACEMENT, FLOOR PLANNING & PIN ASSIGNMENT 9

Simulation base placement algorithms, other placement algorithms - constraint based floor planning - floor planning algorithms for mixed block & cell design - General & channel pin assignment for register minimization, Global routing - Algorithms for global routing.

UNIT IV ROUTING 9

Classification of global routing algorithms - Maze routing algorithm - line probe algorithm - Steiner Tree based algorithms - ILP based approaches-classification of routing algorithms - single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms

UNIT V SYSTEM MODELING ALGORITHMS 9

High level Synthesis - Hardware models - Internal representation - Allocation - Assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of the course, the students will be able to

- Explain the fundamentals of basic algorithm in CAD.
- Analyze the different partitioning algorithm.
- Know about Floor planning and Placement algorithm.
- Understand about different routing algorithms, Modeling and synthesis techniques of CAD.

REFERENCES

- S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley& Sons, 2002.
- N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
- Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World scientific 1999.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	-	3	3	3

PAE15252 **DIGITAL CONTROL ENGINEERING** **3 0 0 3**

COURSE OBJECTIVES

To enable the students to

- impart knowledge on Continuous Time Systems and Controllers
- develop fundamental understanding on Signal Processing in Digital Control
- Study about Design of Digital Control Algorithms
- impart knowledge about State variable Techniques
- give an insight about the Controllability, Observability and Stability

UNIT I CONTINUOUS TIME SYSTEMS 9

Review of frequency and time response analysis and specifications of control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling, time and frequency domain descriptions, aliasing, hold operations, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sample rate, reconstruction, Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems.

UNIT III DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in Z plane

UNIT IV STATE VARIABLE TECHNIQUES 9

Discrete State Variable concepts, Characteristic equation, Eigen values and Eigenvectors, Jordan canonical models, Phase Variable companion forms

UNIT V CONTROLLABILITY, OBSERVABILITY AND STABILITY 9

Definitions and Theorems of Controllability and Observability, Relationships between Controllability, Observability and Transfer Functions, Jury, Routh, Lyapunov stability analysis, Principles of state and output feedback

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand Continuous time System Controllers
- Gain knowledge about Signal Processing in Digital Control
- Design Digital Control Algorithms
- Explain State Variable Techniques
- Know about Controllability, Observability and Stability

REFERENCES

1. Benjamin C.Kuo, "Digital Control Systems", OXFORD University Press, II Edition, 200
2. M.Gopal, "Digital Control and State Variable Methods", Tata McGraw Hill, II Edition, 2007.
3. K.Ogata, "Discrete-Time Control Systems", PHI, II Edition, 2007.
4. Gene. F.Franklin, J.D.Powell, M.Workman, "Digital Control of Dynamic Systems", Addison- Wesley, 1990.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	3	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	3	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	3	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	3	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	3	-	-	-	-	-	-	-	-	3	3	3

PAE15253 **MOBILE NETWORKS** **3 0 0 3**

COURSE OBJECTIVES

To enable the students to

- study architecture and characteristics in cellular networks
- explore enabling wireless technologies with mobile networks
- understand Mobile IP and TCP protocols
- explore issues and challenges in multicast routing in ad-hoc networks

UNIT I CELLULAR CONCEPT **9**

Introduction – Frequency reuse – Channel assignment strategies – Handoff strategies – Interference – Truncking – Improving coverage and capacity in cellular systems.

UNIT II WIRELESS LAN **9**

Infrared vs. radio transmission- Infrastructure and Ad-hoc network – IEEE 802.11 – HIPERLAN –Bluetooth.

UNIT III MOBILE NETWORK LAYER **9**

Mobile IP : Goals – Assumptions and Requirement – Entities – IP packet Delivery- Agent advertisement and Discovery – Registration – Tunneling and Encapsulation – Optimization – Reverse Tunneling – IPv6 – DHCP- Ad hoc Networks

UNIT IV MOBILE TRANSPORT LAYER **9**

Traditional TCP- Indirect TCP- Snooping TCP- Mobile TCP- Fast retransmit/ Fast Recovery- Transmission/ Timeout Freezing – Selective Retransmission- Transaction Oriented TCP , TCP over 2.5/3G wireless networks.

UNIT V MULTICAST ROUTING IN AD-HOC WIRELESS NETWORKS **9**

Introduction – Issues in designing a multicast routing protocol – Operations of multicast routing protocols- Tree based multicast routing protocols – Mesh based multicast routing protocol – Application Dependent multicast routing.

TOTAL PERIODS **45**

COURSE OUTCOMES

At the end of the course, the students will be able to

1. Ability to identify the various challenges and vulnerabilities in cellular networks
2. Understand and recognize techniques of various wireless technologies
3. Analyze the solutions for configuration of mobile networks
4. Explain TCP protocols in mobile environment
5. Analyze the solutions for multicast routing protocols for different applications

REFERENCES

1. Jochen Schiller “Mobile communications”, Pearson Education, New Delhi, Second Edition, 2004.
2. Theodore S Rappaport, “Wireless Communications Principles and Practice”, Pearson Education, New Delhi, Second Edition, 2003.
3. Siva Ram Murthy C and Manoj B S “Ad-hoc Wireless Networks, Architectures and Protocols” Pearson Education, New Delhi, 2005.
4. Charles E Perkins, “Mobile IP: Design Principles and Practice”, Addison Wesley, USA, 1999.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	3	-	3	3
CO2	3	3	-	-	-	-	-	-	-	-	3	-	3	3
CO3	3	3	-	-	-	-	-	-	-	-	3	-	3	3
CO4	3	3	-	-	-	-	-	-	-	-	3	-	3	3
CO5	3	3	-	-	-	-	-	-	-	-	3	-	3	3

PAE15254 **SENSORS AND SIGNAL CONDITIONING** **3 0 0 3**

COURSE OBJECTIVES

To enable the students to

- introduce the basic Science of Measurement
- introduce resistive sensors
- learn the reactive sensors and self-generating sensors
- study about digital sensor and semiconductor device sensors

UNIT I CHARACTERISTICS OF MEASUREMENT SYSTEMS 9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response..

UNIT II RESISTIVE SENSORS 9

Resistive sensors: potentiometers, strain gages and types, resistive temperature detectors (RTDs), thermistors, magneto resistors, light-dependent resistors (LDRs); Signal conditioning for resistive sensors: measurement of resistance, voltage, Wheatstone bridge. Balance and deflection measurements, sensor bridge calibration and compensation instrumentation amplifiers, interference types and reductionry signals.

UNIT III REACTIVE SENSORS 9

Reactance variation and electromagnetic sensors : capacitive sensors – variable & differential, inductive sensors – reluctance variation, eddy current, linear variable differential transformers (LVDTS) , variable transformers: synchros, resolvers, inductosyn , magneto elastic sensors, electromagnetic sensors – sensors based on faraday‟s law, hall effect sensors, Signal conditioning for reactance variation sensors : problems and alternatives, ac bridges, carrier amplifiers – application to the LVDT, variable oscillators, resolver-to- digital and digital-to-resolver converters

UNIT IV MEASURING DEVICES 9

Capacitive Impedance and Piezoelectric Hygrometers - Differential Pressure, U-tube and ultrasonic Densitometers - pH measurement: Ion Selective Type - Radiation Fundamentals-Radiation Detectors- Radiation Thermometers - Optical Pyrometers

UNIT V DIGITAL SENSORS **9**

Position encoders, variable frequency sensors-quartz digital thermometer, SAW sensors, digital flow meters, sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, charge-coupled sensors.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of the course, the students will be able to

- Gain knowledge on basic characteristics of measurement systems
- Know the functionality of resistive sensors and reactive sensors
- Understand the digital sensor and semiconductor device sensors

REFERENCES

Understand the digital sensor and semiconductor device sensors

1. D.Patranabis, “Sensors and Transducers”, TMH 2003.
2. .Jon Wilson, “Sensor Technology Handbook”, Newnes, 2004.
3. Herman K.P. Neubrat, “Instrument Transducers – An Introduction to Their Performance and Design”, Oxford University Press.
4. E.O. Doeblin, “Measurement System: Applications and Design”, McGraw Hill Publications.Analysis",John Wiley, New York, 2000

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	-	-	-	3	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	3	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	3	-	-	-	-	-	3	3	3

PAE15351 **VLSI DESIGN TECHNIQUES** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- study basics of MOS transistor and IC fabrication.
- learn inverters characteristics and logic function.
- learn circuit characterization and performance estimation.
- study VLSI circuits.
- learn Verilog HDL and design VLSI circuits.

UNIT I VLSI DESIGN PROCESS AND MOS TRANSISTOR THEORY 9+6

VLSI Design Process – Architectural Design – Logical Design – Physical Design – Layout Styles –Full custom, Semicustom approaches.MOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model, Non ideal I-V effects, DC transfer characteristics, VLSI Design flow.

UNIT II INVERTERS AND LOGIC GATES 9+6

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9+6

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining, Charge sharing - Scaling

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS 9+6

Multiplexers, Decoders, comparators, priority encoders, Shift registers- Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers.

UNIT V VERILOG HARDWARE LANGUAGE 9+6

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand basics of MOS transistor and IC fabrication, inverters characteristics and logic function.

- Explain circuit characterization and performance estimation.
- Understand the concepts of VLSI circuits.
- Understand Verilog HDL and design VLSI circuits.

REFERENCES

1. Jan M Rabaey, " Digital Integrated Circuits", Prentice Hall of India, 2002
2. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits- Analysis and Design", Tata McGraw Hill, 2003..
3. SamirPalnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4. EugeneD.Fabricius, "Introduction to VLSI Design", McGraw Hill International Editions, 1990.
5. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	3	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	3	3	3	3

PAE15352 **FIBER OPTIC SENSORS** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- understand sensor technology and basic concepts of grating sensor
- know about distributed and magnetic sensor.
- learn about chemical and Biosensors
- study the applications of sensors

UNIT I SENSOR TECHNOLOGY **9+6**

The Emergence of Fiber Optic Sensor Technology-Optical Fibers-Light Sources-Optical Detectors- Optical Modulators- Intensity modulated sensors, Micro bend strain intensity modulated sensor, Liquid level type hybrid sensor, internal effect intensity modulated sensor, Diffraction grating sensors and Interferometric sensors- Fabryperot, Mach Zender, Michelson and Sagnac sensors,

UNIT II GRATING SENSORS **9+6**

Multimode Grating and Polarization Sensors-Sensors Based on Relative Movement of Opposed Gratings-Grating Period Modulation-Sensors Based on the Photo elastic Effect-Retardation Plates- Fiber Grating Sensors

UNIT III DISTRIBUTED AND MAGNETIC SENSORS **9+6**

Fiber Optic distributed and Magnetic Sensor-Distributed Sensing- Basic Principles of Sensor Multiplexing-Interferometric Sensor Multiplexing- Faraday effect sensors- Magneto strictive – Lorentz force sensors- Evanescent Field Absorption Sensors

UNIT IV CHEMICAL AND BIOSENSOR **9+6**

Fiber Optic Chemical and Biosensor: Reagent Mediated sensor-Humidity sensor – pH sensor -Hydrogen sensor - CO2 sensor – Ammonia sensor - Chloride sensor – Glucose sensor – Oxygen sensor - Surface Plasmonic Resonance based sensor

UNIT V APPLICATIONS **9+6**

Industrial Applications of Fiber Optic Sensors : Temperature – Pressure - fluid level – flow – position - vibration - rotation measurements - Current -voltage measurement - Chemical analysis. Introduction to smart structures - Applications –skins

TOTAL PERIODS **45+30**

COURSE OUTCOMES

At the end of the course, the students will be able to

- Know the sensor technology
- Know the sensor concepts of grating sensor
- Know the sensor magnetic sensors.
- Study the application of sensor

REFERENCES

1. Eric Udd, William B. Spillman, Jr., "Fiber Optic Sensors: An Introduction for Engineers and Scientists", John Wiley & Sons 2011
2. Bhagavanadasa Gupta, Banshi Das Gupta, "Fiber Optic Sensors: Principles and Applications", New India Publishing 2006
3. David A. Krohn, "Fiber optic sensors: fundamentals and applications", ISA Publishing 2000
4. Francis T.S. Yu, Shizhuo Yin, Paul B. Ruffin, "Fiber Optic Sensors", CRC Press Publisher, 2010

Mapping of Course Outcomes with Programme Outcomes:
(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	-	3	3	3

PAE15353 WIRELESS COMMUNICATIONS AND MIMO SYSTEMS 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- familiarize the Number systems concept and Arithmetic UNITs
- understand the concepts of Digital signal processing.
- study the concepts & gain knowledge about digital filters.
- study DSP architectures.
- understand the Design of DSP integrated circuit.

UNIT I NUMBER SYSTEMS AND ARITHMETIC UNITS 9+6

Conventional Number system - Redundant Number system - Residue Number System - Bit Parallel and Bit Serial Arithmetic - Distributed arithmetic - Basic Shift Accumulator - Reducing the memory size - Complex multipliers - improved shift-Accumulator

UNIT II DIGITAL SIGNAL PROCESSING 9+6

Digital signal processing, Sampling of analog signals - Selection of sample frequency - Signal-processing systems - Frequency response - Transfer functions - Signal flow graphs - Filter structures - Adaptive DSP algorithms - DFT-The Discrete Fourier Transform - FFT-The Fast Fourier Transform Algorithm, Image coding - Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9+6

FIR filters - FIR filter structures - FIR chips - IIR filters - Specifications of IIR filters - Mapping of analog transfer functions - Mapping of analog filter structures - Multirate systems - Interpolation with an integer factor L - Sampling rate change with a ratio L/M - Multirate filters - Finite word length effects -Parasitic oscillations - Scaling of signal levels - Round-off noise- measuring round-off noise- Coefficient sensitivity- Sensitivity and noise

UNIT IV DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9+6

Standard digital signal processors - Application specific IC‟s for DSP - DSP systems - DSP system design - Integrated Circuits design - MOS transistors - MOS Logic - VLSI Process technologies - Trends in CMOStechnologies

UNIT V DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9+6

DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multicomputers - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit – serial PEs.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand the concepts of DSP
- Design digital filters and understand the finite word length effects in the same
- Understand DSP architectures.
- Explain DSP integrated circuit and VLSI circuit technologies

REFERENCES

1. Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York 1999.
2. A.V.Oppenheim et.al, “Discrete-time Signal Processing”, Pearson education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, “Digital signal processing A practical approach”, Second edition, Pearson education, Asia 2001.
4. Keshab K. Parhi, “VLSI digital Signal Processing Systems design and Implementation”, John Wiley& Sons, 1999.
5. Bayoumi & Magdy A., “VLSI Design Methodologies for Digital Signal Processing Architectures”, BS Publications, 2005..

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	-	-	-	3	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	3	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	3	-	-	-	-	-	3	3	3

PAE15354 **RF SYSTEM DESIGN** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- learn RF design and circuit board components
- understand various impedance transformers and biasing networks
- study the basic RF components
- acquire knowledge of RF filters and RF synthesizer.
- study the basic RF mixers and oscillators

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES **9+6**

CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct up conversion, Two step up conversion..

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS **9+6**

S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancementHigh frequency amplifier design Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS **9+6**

Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation Power Amplifiers: General model – Class A, AB, B, C, D, E and F amplifiers – Linearization Techniques – Efficiency boosting techniques – ACPR metric – Design considerations..

UNIT IV PLL AND FREQUENCY SYNTHESIZERS **9+6**

PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers.

UNIT V MIXERS AND OSCILLATORS **9+6**

Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – sub sampling mixers Oscillators: Describing Functions, Colpitt‟s oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise.

TOTAL PERIODS **45+30**

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand various RF issues.
- Gain Knowledge on impedance transformation.
- Know about active RF component, matching and biasing networks
- Understand the concepts of RF filter design and their implementation using software.
- Explain the operation of RF oscillators and mixers and their design.

REFERENCES

1. T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.
2. Reinhold Ludwig and Powel Bretchko, "RF Circuit Design – Theory and Applications", Pearson Education Asia, 2006
3. Kai Chang, InderBahl and Vijay Nair, "RF and Microwave Circuit and Component Design for Wireless Systems", John Wiley and Sons, 2002.
4. Jan Crols, MichielSteyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997
5. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001.

Mapping of Course Outcomes with Programme Outcomes:

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COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	-	3	3	3

PAE15451 **PHYSICAL DESIGN OF VLSI CIRCUITS** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- gain knowledge of basic rules of layout and cell generations.
- study about the placement and floor sizing.
- learn about the multiple partition, routing and how to increases the layout performance.
- improve the performance in the layout design.
- acquire knowledge about Cell Partition and generation.

UNIT I REVIEW OF VLSI TECHNOLOGY **9+6**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity- Algorithmic Paradigms

UNIT II PLACEMENT USING TOP-DOWN APPROACH **9+6**

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut- partition with capacity and i/o constraints. Floor planning: Rectangular dual floor planning- hierarchical approach simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH **9+6**

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches hierarchical approaches- multi commodity flow based techniques- Randomized Routing- One Step approach- Integer Linear Programming Detailed Routing: Channel Routing- Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT **9+6**

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization.

UNIT V LAYOUT DESIGN AND TOOLS **9+6**

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

TOTAL PERIODS **45+30**

COURSE OUTCOMES

At the end of the course, the students will be able to

- Design, simulate, built on an abstract functional specification.
- Partition the layout easily for the design of PCB Boards in accurate manner using many approaches.
- Discover the debug complex combinational and sequential circuits based on an abstract functional specification.
- Perform the cell partition and generation.
- Learn about the routing of the cell.

REFERENCES

1. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill International Edition 1995
2. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.
3. Jose E. France and Yannis T sividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
4. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press , 2003

Mapping of Course Outcomes with Programme Outcomes:

(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak

COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO2	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO3	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	-	-	-	-	-	-	-	-	-	3	3	3
CO5	3	3	-	-	-	-	-	-	-	-	-	3	3	3

PAE15452 **VLSI SIGNAL PROCESSING** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- understand the basic concepts of DSP algorithms.
- know about the Folding & unfolding concepts.
- analyze the various pipelining and parallel processing techniques.
- analyze the retiming and unfolding algorithms for various DSP applications.
- Analyze the concept of various filters

UNIT I INTRODUCTION TO DSP SYSTEMS **9+6**

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING, FOLDING AND UNFOLDING **9+6**

Retiming - definitions and properties Retiming techniques; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Folding – Folding transformation – Register minimizing techniques – Register minimization in folded architectures.

UNIT III FAST CONVOLUTION **9+6**

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm –Iterated Convolution – Cyclic Convolution; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT–LEVEL ARCHITECTURE AND SYSTOLIC ARRAY DESIGN **9+6**

Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh- Wooley carry-save multiplication tabular form and implementation, design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement. Systolic array design methodology – FIR systolic Arrays – selection of scheduling vector-matrix multiplication and 2D systolic array design-Systolic design for space representations containing Delays

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS **9+6**

Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in

edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Understand the basic concepts of DSP algorithms.
- Analyze pipelining and other parallel processing techniques
- Perform digital signal processor programming.

REFERENCES

1. KeshabK.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
3. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw- Hill, 1994.
4. Jose E. France and Yannis T sividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
5. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.

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COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	3	-	-	-	-	-	-	-	3	3	3	3
CO2	3	3	3	-	-	-	-	-	-	-	3	3	3	3
CO3	3	3	3	-	-	-	-	-	-	-	3	3	3	3
CO4	3	3	3	-	-	-	-	-	-	-	3	3	3	3
CO5	3	3	3	-	-	-	-	-	-	-	3	3	3	3

PAE15453 SOLID STATE DEVICE MODELING AND SIMULATION 3 2 0 4

COURSE OBJECTIVES

To enable the students to

- understand the basic semiconductor physics,
- understand basic concepts bipolar device modeling
- understand the operation of MOSFET modeling
- study the parameter measurement and optoelectronic device modeling

UNIT I BASIC SEMICONDUCTOR PHYSICS 9+6

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources - Diodes : Forward and Reverse biased junctions – Reverse bias breakdown – Transient and AC conditions –– Static and Dynamic behavior- Small and Large signal models – SPICE model for a Diode – Temperature and Area effects on Diode Model Parameters.

UNIT II BIPOLAR DEVICE MODELING 9+6

Transistor Models: BJT – Transistor Action – Minority carrier distribution and Terminal currents - Switching- Eber - Molls and Gummel Poon Model, SPICE modeling - temperature and area effects.

UNIT III MOSFET MODELING 9+6

OS Transistor – NMOS, PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT IV PARAMETER MEASUREMENT 9+6

Bipolar Junction Transistor Parameter – Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques, Gunmel Plots, MOSFET: Long and Short Channel Parameters, Measurement ofCapacitance.

UNIT V OPTOELECTRONIC DEVICE MODELING 9+6

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

TOTAL PERIODS 45+30

COURSE OUTCOMES

At the end of the course, the students will be able to

- Know the fundamental of physics and BJT modeling

- Understand MOSFET modeling and optoelectronic Device Modeling
- Explain parameter measurement

REFERENCES

1. Ben.G..Streetman, “Solid State Devices”, Prentice Hall, 1997.
2. Giuseppe Massobrio and Paolo Antogentti, “Semiconductor Device Modeling with SPICE” Second Edition, McGraw-Hill Inc, New York, 1993.
3. Tyagi M.S. “Introduction to Semiconductor Devices”, 2nd Edition McGraw Hill, New York, 1981.
4. S.M.Sze “Semiconductor Devices - Physics and Technology”, John Wiley and sons, 1985.
5. Mohammed Ismail & Terri Fiez “Analog VLSI-Signal & Information Processing” 1stED, Tata McGraw Hill Publishing company Ltd 2001.

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COs	**Programme Outcomes(POs)**													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	3	-	-	-	-	-	-	-	3	-	3	3
CO2	3	3	3	-	-	-	-	-	-	-	3	-	3	3
CO3	3	3	3	-	-	-	-	-	-	-	3	-	3	3
CO4	3	3	3	-	-	-	-	-	-	-	3	-	3	3
CO5	3	3	3	-	-	-	-	-	-	-	3	-	3	3

PAE15454 **HIGH PERFORMANCE NETWORKS** **3 2 0 4**

COURSE OBJECTIVES

To enable the students to

- develop a comprehensive understanding of multimedia networking applications
- study the types of VPN and tunneling protocols for security..
- learn about network security in many layers and network management.
- understand various Network security and management

UNIT I SWITCHING AND ROUTING **9+6**

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing - SONET –DWDM – DSL – ISDN – BISDN, ATM, Architecture of 802.11

UNIT II MULTIMEDIA NETWORKING APPLICATIONS **9+6**

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services –RSVP- differentiated services.

UNIT III ADVANCED NETWORKS CONCEPTS **9+6**

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks- P2P connections.

UNIT IV CONGESTION AND TRAFFIC MODELING **9+6**

Effects of congestion, Congestion control, Little‟s theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, ABR traffic management, GBR traffic Management, Network performance evaluation.

UNIT V NETWORK SECURITY AND MANAGEMENT **9+6**

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL PERIODS **45+30**

COURSE OUTCOMES

- At the end of the course, the students will be able to
- Gain a comprehensive understanding on multimedia networking applications
- Know about the types of VPN and tunneling protocols for security
- Understand the various ways of controlling the traffic and its methods
- Explain network security in many layers and network management

REFERENCES

1. J.F. Kurose & K.W. Ross, "Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003.
2. Aunuragkumar, D. M Anjunath, Joy kuri, "Communication Networking", Morgan Kaufmann Publishers, 1ed 2004
3. HersentGurle& petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003.
4. Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet" fifth edition, Pearson education 2006.
5. Nader F.Mir, "Computer and Communication Networks", first edition, 2010

Mapping of Course Outcomes with Programme Outcomes:

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COs	Programme Outcomes(POs)													
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
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CO2	3	3	3	-	-	-	-	-	-	-	3	3	3	3
CO3	3	3	3	-	-	-	-	-	-	-	3	3	3	3
CO4	3	3	3	-	-	-	-	-	-	-	3	3	3	3
CO5	3	3	3	-	-	-	-	-	-	-	3	3	3	3

AP7301	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the basics of EMI
- To study EMI Sources
- To understand EMI problems
- To understand Solution methods in PCB
- To understand Measurement technique for emission
- To understand Measurement technique for immunity

UNIT I EMI/EMC CONCEPTS **9**

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES **9**

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES **9**

Shielding- Shielding Material-Shielding integrity at discontinuities, Filtering- Characteristics of Filters-Impedance and Lumped element filters-Telephone line filter, Power line filter design, Filter installation and Evaluation, Grounding- Measurement of Ground resistance-system grounding for EMI/EMC-Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control. EMI gaskets

UNIT IV EMC DESIGN OF PCBS **9**

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits ,Component selection and mounting; PCB trace impedance; Routing; Cross talk control-Electromagnetic Pulse-Noise from relays and switches, Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS **9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Frequency assignment - spectrum conversation. British VDE standards, Euro norms standards in japan - comparisons. EN Emission and Susceptibility standards and Specifications.

TOTAL: 45PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- To design a EMI free system
- To reduce system level crosstalk
- To design high speed Printed Circuit board with minimum interference
- To make our world free from unwanted electromagnetic environment

REFERENCES:

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996
2. Clayton R.Paul,” Introduction to Electromagnetic Compatibility”, John Wiley Publications, 2008
3. Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, New york, 1988.
4. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Norwood, 1986.
5. Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC”, Vol I-V, 1988.

DS7201 ADVANCED DIGITAL IMAGE PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To understand the image fundamentals and mathematical transforms necessary for image processing and to study the image enhancement techniques.
- To understand the image segmentation and representation techniques.
- To understand how image are analyzed to extract features of interest.
- To introduce the concepts of image registration and image fusion.
- To analyze the constraints in image processing when dealing with 3D data sets.

UNIT I FUNDAMENTALS OF DIGITAL IMAGE PROCESSING 9

Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency domain, Review of morphological image processing

UNIT II SEGMENTATION 9

Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour methods, Texture feature based segmentation, Model based segmentation, Atlas based segmentation, Wavelet based Segmentation methods

UNIT III FEATURE EXTRACTION 9

First and second order edge detection operators, Phase congruency, Localized feature extraction-detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features

UNIT IV REGISTRATION AND IMAGE FUSION 9

Registration- Preprocessing, Feature selection-points, lines, regions and templates Feature correspondence-Point pattern matching, Line matching, region matching Template matching .Transformation functions-Similarity transformation and Affine Transformation. Resampling- Nearest Neighbour and Cubic Splines Image Fusion-Overview of image fusion, pixel fusion, Multiresolution based fusion discrete wavelet transform, Curvelet transform. Region based fusion.

REFERENCES:

1. J.F. Kurose & K.W. Ross,"Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003.
2. Walrand .J. Varatya, High performance communication network, Morgan Kauffman – Harcourt Asia Pvt. Ltd. 2nd Edition, 2000.
3. LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.
4. Aunurag kumar, D. M Anjunath, Joy kuri, "Communication Networking", Morgan Kaufmann Publishers, 1ed 2004.
5. Hersent Gurle & petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003.
6. Fred Halsall and Lingana Gouda Kulkarni,"Computer Networking and the Internet" fifth edition, Pearson education 2006
7. Nader F.Mir ,Computer and Communication Networks, first edition 2010
8. Larry l.Peterson & Bruce S.David, "Computer Networks: A System Approach"- 1996.

VL7301 **TESTING OF VLSI CIRCUITS** **L T P C**
3 0 0 3

OBJECTIVES:

- To know the various types of faults and also to study about fault detection, dominance
- To know the concepts of the test generation methods-DFT-BIST.
- To understand the fault diagnosis methods.

UNIT I TESTING AND FAULT MODELLING **9**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION **9**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY **9**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS **9**

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS **9**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

TOTAL: 45 PERIODS

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

VL7013 VLSI FOR WIRELESS COMMUNICATION L T P C
3 0 0 3

OBJECTIVES:

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication.

UNIT I COMPONENTS AND DEVICES 9

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

UNIT II MIXERS 9

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise - A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT III FREQUENCY SYNTHESIZERS 9

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT IV SUB SYSTEMS 9

Data converters in communications, adaptive Filters, equalizers and transceivers

UNIT V IMPLEMENTATIONS 9

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System.

TOTAL: 45PERIODS

REFERENCES:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.
4. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2000.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
6. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.

AP7011 PHOTONICS L T P C
3 0 0 3

OBJECTIVES:

- To gain knowledge about light and its propagation.
- To study the different types of laser and its effects.
- To learn about holography.
- To study the non-linear optic devices.

UNIT I INTRODUCTION TO PHOTONICS 9

Nature of Light – Wave and light terminology, Maxwell equation, light spectra and sources, absorption and emission, black body radiation. Geometric Optics – Light as a ray, law of reflection including plane mirrors, law of refraction including optical fiber applications, prisms and thin lenses including Lensmaker's equation, Lens problems and optical instruments using the thin lens equation.

UNIT II WAVE OPTICS 9

Wave descriptive terminology, wave superposition (interference) including double – slit interference, diffraction and diffraction gratings, interference applications, eg. Michelson, Mach Zender and Fabry Perot interferometers, Thin film interference and Fiber Bragg Gratings. Diffraction Effects including: airy disk, near far field effects. Polarization principles including scattering, reflection and birefringence.

UNIT III LASERS 9

Introduction to Lasers – Basic terminology and theory of operation including specific requirements, principal types of lasers. Laser radiation hazards including effects on the eye and skin. Laser safety standards and hazard classifications. Laser safety precautions and protective measures

UNIT IV HOLOGRAPHY 9

Holography – Theory and basic principles, Requirement to record and reconstruct holograms – Experimental techniques- Recording Materials-Reflection holography and applications-Holographic interoferrometry-Nondestructive testing, optical memory."

UNIT V NON-LINEAR OPTICS 9

Non-linear optics – Harmonic Generation, sum and difference frequency generation, wave mixing, Optical Parametric Oscillator. Non-linear optic materials – inorganic and organic. Phase matching, efficiency of harmonic generation- powder and single crystal methods. Methods of determination of harmonic coefficients – Z-scan and Electrical Field Induced Second Harmonic. Phase conjugation-Silicon Photonics-Silicon on Insulator Photonics-Fabrication of Silicon Waveguides"

TOTAL: 45 PERIODS

REFERENCES:

1. Bahaa E. A. Saleh, Malvin Carl Teich, "Fundamentals of Photonics", John Wiley & Sons 2011
2. T.P. Pearsall, "Photonics Essentials: An introduction with experiments", McGraw Hill 2003
3. F.G. Smit and T.A. King, "Optics and Photonics: An introduction", Wiley & Sons, Ltd 2003
4. B. Balkrishna Laud, "Lasers and Non-Linear Optics", New Age International 2011
5. R.S. Quimby, "Photonics and Lasers-An Introduction", Wiley 2006
6. R. Menzel, "Photonics", Springer-Verlag 2007
7. F.A. Jenkins and H.E. White, "Fundamentals of Optics", McGraw Hill 1976
8. Yariv Yeh and Pochi Yeh, "Photonics – Optical Electronics in Modern Communications", 6th Eition, Oxford University Press 2012
9. Abdul Al-Azzawi, "Photonics: Principles and Practices", CRC Press 2007
10. Graham T. Reed, Andrew P. Knights, "Silicon Photonics: An Introduction", John Wiley & Sons 2004.

AP7012 NANO ELECTRONICS L T P C
3 0 0 3

OBJECTIVES:

- To learn and understand basic concepts of Nano electronics.
- To know the techniques of fabrication and measurement.
- To gain knowledge about Nanostructure devices and logic devices.

UNIT I INTRODUCTION TO NANOELECTRONICS 9

Microelectronics towards biomolecule electronics-Particles and waves- Wave-particle duality- Wave mechanics- Schrödinger wave equation- Wave mechanics of particles: - Atoms and atomic orbitals- Materials for nanoelectronics- Semiconductors- Crystal lattices: Bonding in crystals- Electron energy bands- Semiconductor heterostructures- Lattice-matched and pseudomorphic heterostructures- Inorganic-organic heterostructures- Carbon nanomaterials: nanotubes and fullerenes

UNIT II FABRICATION AND MEASUREMENT TECHNIQUES 9

Growth, fabrication, and measurement techniques for nanostructures- Bulk crystal and heterostructure growth- Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices- Techniques for characterization of nanostructures- Spontaneous formation and ordering of nanostructures- Clusters and nanocrystals- Methods of nanotube growth- Chemical and biological methods for nanoscale fabrication- Fabrication of nano-electromechanical systems

UNIT III PROPERTIES 9

Dielectrics-Ferroelectrics-Electronic Properties and Quantum Effects-Magnetoelectronics – Magnetism and Magnetotransport in Layered Structures-Organic Molecules – Electronic Structures, Properties, and Reactions-Neurons – The Molecular Basis of their Electrical Excitability-Circuit and System Design- Analysis by Diffraction and Fluorescence Methods-Scanning Probe Techniques

UNIT IV NANO STRUCTURE DEVICES 9

Electron transport in semiconductors and nanostructures- Time and length scales of the electrons in solids- Statistics of the electrons in solids and nanostructures- Density of states of electrons in nanostructures- Electron transport in nanostructures-Electrons in traditional low-dimensional structures- Electrons in quantum wells- Electrons in quantum wires- Electrons in quantum dots- Nanostructure devices- Resonant-tunneling diodes- Field-effect transistors- Single-electron-transfer devices- Potential-effect transistors- Light-emitting diodes and lasers- Nano-electromechanical system devices- Quantum-dot cellular automata

UNIT V LOGIC DEVICES AND APPLICATIONS 9

Logic Devices-Silicon MOSFETs-Ferroelectric Field Effect Transistors-Quantum Transport Devices Based on Resonant Tunneling-Single-Electron Devices for Logic Applications-Superconductor Digital Electronics-Quantum Computing Using Superconductors-Carbon Nanotubes for Data Processing-Molecular Electronics

TOTAL: 45PERIODS

REFERENCES:

1. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press 2011
2. Supriyo Datta,"Lessons from Nanoelectronics: A New Perspective on Transport", World Scientific 2012
3. George W. Hanson,"Fundamentals of Nanoelectronics", Pearson 2009
4. Korkin, Anatoli; Rosei, Federico (Eds.), "Nanoelectronics and Photonics",Springer 2008
5. Mircea Dragoman, Daniela Dragoman, "Nanoelectronics: principles and devices", CRC Press 2006
6. Karl Goser, Peter Glösekötter, Jan Dienstuhl,"Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices", Springer 2004
7. W. R. Fahrner, Nanotechnology and Nan electronics: Materials, Devices, Measurement Techniques (SpringerVerlag Berlin Heidelberg 2005)
8. Mark A. Reed, Takhee Lee,"Molecular nanoelectronics", American Scientific Publishers 2003
9. Jaap Hoekstra, "Introduction to Nanoelectronic Single-Electron Circuit Design", Pan Stanford Publishing 2010
10. W. Ranier, "Nano Electronics and Information Technology", John Wiley & Sons 2012

AP7013 PATTERN RECOGNITION L T P C
3 0 0 3

OBJECTIVES:

- To know about Supervised and unsupervised Learning.
- To study about feature extraction and structural pattern recognition.
- To explore different classification models.
- To understand Fuzzy Pattern Classifiers and Perception.

UNIT I PATTERN CLASSIFIER 9

Overview of Pattern recognition – Discriminant functions – Supervised learning – Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter Estimation – Problems with Bayes approach– Pattern classification by distance functions – Minimum distance pattern classifier.

UNIT II CLUSTERING 9

Clustering for unsupervised learning and classification – Clustering concept – C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UINT III FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION 9

KL Transforms – Feature selection through functional approximation – Binary selection -Elements of formal grammars - Syntactic description - Stochastic grammars - Structural representation. .

UNIT IV HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE 9

State Machines – Hidden Markov Models – Training – Classification – Support vector Machine – Feature Selection.

UNIT V RECENT ADVANCES **9**

Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception.

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Classify the data and identify the patterns.
- Extract feature set and select the features from given data set.

REFERENCES:

1. M. Narasimha Murthy and V. Susheela Devi, "Pattern Recognition", Springer 2011.
2. S.Theodoridis and K.Koutroumbas, "Pattern Recognition", 4th Ed., Academic Press, 2009.
3. Robert J.Schalkoff, "Pattern Recognition Statistical, Structural and Neural Approaches", John Wiley & Sons Inc., New York, 1992.
4. C.M.Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.
5. R.O.Duda, P.E.Hart and D.G.Stork, "Pattern Classification", John Wiley, 2001
6. Andrew Webb, "Stastical Pattern Recognition", Arnold publishers, London,1999.

AP7014 OPTICAL COMPUTING **L T P C**
3 0 0 3

OBJECTIVES:

- To know the basic pricinciples of optical computing.
- To study about various optical computing elements.
- To study and compare analog and digital optical computing.

UNIT I OPTICAL COMPUTING PRINCIPLES **9**

Non Von-Neuman architecture, various forms of parallel processing, SLM, LEDs, Lasers and Photo detectors arrays, Holographic techniques, Optical storage devices.

UNIT II DIGITAL LOGIC **9**

Symbolic substitution, Image computing, Cellular logic, Boolean logic, Cellular arrays, Cellular hyper cubes, conventional hyper cube, Binary stack coded arithmetic, Binary Row coded, Binary symbol, Coded arithmetic multilevel logic processing.

UNIT III OPTICAL COMPUTING ELEMENTS **9**

ß switches, Machzender interferometeric logic elements for Boolean functions, Acousto optic; optical matrix multipliers, Non linear optical switches as memories.

UNIT IV ANALOG OPTICAL COMPUTING **9**

Linear optic processing, Analog optical arithmatics. Recognition by analog optical system.

UNIT V DIGITAL OPTICAL COMPUTING **9**

Devices, Shadow casting, Symbolic substitution, Optical matrix processing, Optical linear neural network. Nonlinear network.

TOTAL: 45PERIODS

REFERENCES:

1. A.Karim Mohammed and A.S.Abdul Awwall, Optical computing-An introduction, John Wiley, New York, 1992.
2. Mc. Aulay Alastair.D, Optical Computer Architecture: The Application of optical concepts to next generation computers, John Wiley, New York, 1991.
3. Dror Feitelsen, Optical Computing, MIT press, Cambridge, 1988.

CP7030 ROBOTICS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To understand robot locomotion and mobile robot kinematics
- To understand perception in robotics
- To understand mobile robot localization
- To understand mobile robot mapping
- To understand simultaneous localization and mapping (SLAM)
- To understand robot planning and navigation

UNIT I LOCOMOTION AND KINEMATICS 9

Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability

UNIT II ROBOT PERCEPTION 9

Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data

UNIT III MOBILE ROBOT LOCALIZATION 9

Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments

UNIT IV MOBILE ROBOT MAPPING 9

Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM – extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fastSLAM algorithm

UNIT V PLANNING AND NAVIGATION 9

Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Explain robot locomotion
- Apply kinematics models and constraints
- Implement vision algorithms for robotics
- Implement robot localization techniques
- Implement robot mapping techniques
- Implement SLAM algorithms
- Explain planning and navigation in robotics

REFERENCES:
1. Roland Seigwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, “Introduction to autonomous mobile robots”, Second Edition, MIT Press, 2011.
2. Sebastian Thrun, Wolfram Burgard, and Dieter Fox, “Probabilistic Robotics”, MIT Press, 2005.
3. Howie Choset et al., “Principles of Robot Motion: Theory, Algorithms, and Implementations”, A Bradford Book, 2005.
4. Gregory Dudek and Michael Jenkin, “Computational Principles of Mobile Robotics”, Second Edition, Cambridge University Press, 2010.
5. Maja J. Mataric, “The Robotics Primer”, MIT Press, 2007.

AP7015 OPTICAL IMAGING TECHNIQUES L T P C
3 0 0 3

OBJECTIVES:
- To learn the fundamentals of optical image formation and fourier optics.
- To study and compare coherent and incoherent optical imaging.
- To know the various techniques in the construction of image.

UNIT I FUNDAMENTALS 9
Coherance and light source – optical image formation – Franhoufer diffraction – Single slit – double slit circular aperture – double aperture gratings – 1D and 2D lens aperture – Interference.

UNIT II FOURIER SERIES AND TRANSFORM 9
Fourier series – Fourier coefficients – optical and crystal diffraction gratings – Fourier series formulation – Fourier transform and single slit diffraction – grating pattern – Fourier transform of light waves – correlation.

UNIT III OPTICAL IMAGING AND PROCESSING 9
Incoherent optical imaging – transfer function – coherent optical imaging – periodic and non periodic objects – optical transform – Holography – coherent and incoherent optical processing.

UNIT IV IMAGE CONSTRUCTION TECHNIQUES 9
X – ray computed tomography – reconstruction by simple back projection – iterative reconstruction – analysis methods – magnetic resonance imaging – Ultrasonic computed tomography.

UNIT V APPLICATIONS 9
Michelsons stellar interferometry – spectral interferometer – fringe visibility and spectral distribution – partial coherence and correlation – Fourier transform spectroscopy – Synthetic aperture radar – Intensity interferometer – Imaging by holographic techniques.

TOTAL: 45 PERIODS .

REFERENCES:
1. E.G. Stewart, “Fourier Optics an Introduction”, 2nd Edition, Ellis Harwood limited, Chichester, 1987.
2. Dror.G. Feitelson, “Optical Computing”, MIT press, Cambridge, 1988.

CU7002 **MEMS AND NEMS** **L T P C**
3 0 0 3

OBJECTIVES:

- To introducing the concepts of microelectromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To introducing concepts of quantum mechanics and nano systems.

UNIT I OVERVIEW AND INTRODUCTION 9

New trends in Engineering and Science: Micro and Nanoscale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Microelectromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT III MICRO SENSORS 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor

UNIT IV MICRO ACTUATORS 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits

TOTAL: 45PERIODS

REFERENCES:

1. Marc Madou, “Fundamentals of Microfabrication”, CRC press 1997.
2. Stephen D. Senturia,” Micro system Design”, Kluwer Academic Publishers,2001
3. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.
4. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006,
5. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press, 2002

DS7301 SPEECH AND AUDIO SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To study the basic concepts of speech and audio.
- To study the analysis of various M-band filter banks for audio coding
- To learn various transform coders for audio coding.
- To study the speech processing methods in time and frequency domain

UNIT I MECHANICS OF SPEECH AND AUDIO 9

Introduction - Review Of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking-Nonsimultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

UNIT II TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS 9

Introduction -Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters- Tree-Structured QMF and CQF M-band Banks - Cosine Modulated "Pseudo QMF" M-band Banks - Cosine Modulated Perfect Reconstruction (PR) M-band Banksand the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies.

UNIT III AUDIO CODING AND TRANSFORM CODERS 9

LosslessAudioCoding-LossyAudioCoding- ISO-MPEG-1A,2A,2A Advaned , 4A udioCoding - Optimum Coding in the Frequency Domain - Perceptual Transform Coder -Brandenburg-Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding -Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization -MDCT with Vector Quantization.

UNIT IV TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING 9

Time domain parameters of Speech signal – Methods for extracting the parameters :Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCRand energy
Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods **HOMOMORPHIC SPEECH ANALYSIS:**
Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

UNIT V LINEAR PREDICTIVE ANALYSIS OF SPEECH 9

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.

TOTAL: 45PERIODS

REFERENCES:

1. Digital Audio Signal Processing, Second Edition, Udo Zölzer**,** A John Wiley& sons Ltd Publicatioons
2. Applications of Digital Signal Processing to Audio And Acoustics Mark Kahrs, Karlheinz Brandenburg, KLUWER ACADEMIC PUBLISHERS NEW YORK, BOSTON, DORDRECHT, L ONDON , MOSCOW
3. Digital Processing of Speech signals – L.R.Rabiner and R.W.Schaffer - Prentice Hall –1978

AP7016 **SYSTEM ON CHIP DESIGN** **L T P C**
3 0 0 3

OBJECTIVES :

- To design combinational and sequential logic networks.
- To learn optimization of power in combinational and sequential logic machines.
- To study the design principles of FPGA and PLA.
- To learn various floor planning methods for system design.

UNIT I LOGIC GATES **9**

Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect.

UNIT II COMBINATIONAL LOGIC NETWORKS **9**

Introduction. Standard Cell-Based Layout. Simulation. Combinational Network Delay. Logic and interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.

UNIT III SEQUENTIAL MACHINES **9**

Introduction. Latches and Flip-Flops. Sequential Systems and Clocking Disciplines. Sequential System Design. Power Optimization. Design Validation. Sequential Testing.

UNIT IV SUBSYSTEM DESIGN **9**

Introduction. Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers. High-Density Memory. FieldProgrammable Gate Arrays. Programmable Logic Arrays. References. Problems.

UNIT V FLOOR-PLANNING **9**

Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, The I/O Architecture, PAD Design.

TOTAL: 45PERIODS

REFERENCES:

1. Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition 2008.
2. Wayne Wolf, “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition , 2008.

CP7023 **RECONFIGURABLE COMPUTING** **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the need for reconfigurable computing
- To expose the students to various device architectures
- To examine the various reconfigurable computing systems
- To understand the different types of compute models for programming reconfigurable architectures
- To expose the students to HDL programming and familiarize with the development environment
- To expose the students to the various placement and routing protocols
- To develop applications with FPGAs

UNIT I DEVICE ARCHITECTURE 9

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

UNIT II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 9

Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing.

UNIT IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bitstream Generation – Case Studies with Appropriate Tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9

Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs.

TOTAL: 45 PERIODS

OUTCOMES:

Upon completion of the course, the students will be able to

- Identify the need for reconfigurable architectures
- Discuss the architecture of FPGAs
- Point out the salient features of different reconfigurable architectures
- Build basic modules using any HDL
- Develop applications using any HDL and appropriate tools
- Design and build an SoPC for a particular application

REFERENCES:

1. Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
2. Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, “Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications”, Springer, 2010.

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UNIT I ADHOC NETWORKS AND ROUTING PROTOCOLS 9

Ad hoc Wireless Networks – What is an Ad Hoc Network? Heterogeneity in Mobile Devices – Wireless Sensor Networks – Traffic Profiles – Types of Ad hoc Mobile Communications – Types of Mobile Host Movements – Challenges Facing Ad hoc Mobile Networks – Ad hoc wireless Internet .

Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks – Classifications of Routing Protocols – Table–Driven Routing Protocols – Destination Sequenced Distance Vector (DSDV) – Wireless Routing Protocol (WRP) – Cluster Switch Gateway Routing (CSGR) – Source–Initiated On–Demand Approaches – Ad hoc On–Demand Distance Vector Routing (AODV) – Dynamic Source Routing (DSR) –Temporally Ordered Routing Algorithm (TORA) – Signal Stability Routing (SSR) – Location–Aided Routing (LAR) – Power–Aware Routing (PAR) – Zone Routing Protocol (ZRP).

UNIT II MULTICAST ROUTING AND SECURITY 9

Issues in Designing a Multicast Routing Protocol – Operation of Multicast Routing Protocols – An Architecture Reference Model for Multicast Routing Protocols –Classifications of Multicast Routing Protocols – Tree–Based Multicast Routing Protocols– Mesh–Based Multicast Routing Protocols – Summary of Tree and Mesh based Protocols – Energy–Efficient Multicasting – Multicasting with Quality of Service Guarantees – Application – Dependent Multicast Routing –

Comparisons of Multicast Routing Protocols - Design Goals of a Transport Layer Protocol for Ad hoc Wireless Networks –Classification of Transport Layer Solutions – TCP over Ad hoc Wireless Networks- Security in Ad Hoc Wireless Networks – Network Security Requirements – Issues and Challenges in Security Provisioning – Network Security Attacks – Key Management – Secure Routing in Ad hoc Wireless Networks.

UNIT III QoS AND ENERGY MANAGEMENT 9

Issues and Challenges in Providing QoS in Ad hoc Wireless Networks – Classifications of QoS Solutions – MAC Layer Solutions – Network Layer Solutions – QoS Frameworks for Ad hoc Wireless Networks Energy Management in Ad hoc Wireless Networks – Introduction – Need for Energy Management in Ad hoc Wireless Networks – Classification of Energy Management Schemes – Battery Management Schemes – Transmission Power Management Schemes – System Power Management Schemes.

UNIT IV SENSOR NETWORKS – ARCHITECTUREAND MACPROTOCOLS 9

Single node architecture – Hardware components, energy consumption of sensor nodes, Network architecture – Sensor network scenarios, types of sources and sinks, single hop versus multi-hop networks, multiple sinks and sources, design principles, Development of wireless sensor networks. , physical layer and transceiver design consideration in wireless sensor networks, Energy usage profile, choice of modulation, Power Management - MAC protocols – fundamentals of wireless MAC protocols, low duty cycle protocols and wakeup concepts, contention-based protocols, Schedule-based protocols - SMAC, BMAC, Traffic-adaptive medium access protocol (TRAMA), Link Layer protocols – fundamentals task and requirements, error control, framing, link management.

UNIT V SENSOR NETWORKS – ROUTING PROTOCOLS AND OPERATING SYSTEMS 9

Gossiping and agent-based uni-cast forwarding, Energy-efficient unicast, Broadcast and multicast, geographic routing, mobile nodes, Data-centric routing – SPIN, Directed Diffusion, Energy aware routing, Gradient-based routing – COUGAR, ACQUIRE, Hierarchical Routing – LEACH, PEGASIS, Location Based Routing – GAF, GEAR, Data aggregation – Various aggregation techniques. Introduction to TinyOS – NesC, Interfaces, modules, configuration, Programming in TinyOS using NesC, Emulator TOSSIM.

TOTAL: 45 PERIODS

REFERENCES:

1. C. Siva Ram Murthy and B. S. Manoj, “Ad Hoc Wireless Networks Architectures and Protocols”, Prentice Hall, PTR, 2004.
2. C. K. Toh, “Ad Hoc Mobile Wireless Networks Protocols and Systems”, Prentice Hall, PTR, 2001.
3. Charles E. Perkins, “Ad Hoc Networking”, Addison Wesley, 2000.
4. Kazem Sohraby, Daniel Minoli and Taieb Znati, “ Wireless Sensor Networks Technology-Protocols and Applications”, John Wiley & Sons, 2007.
5. Feng Zhao, Leonidas Guibas, “Wireless Sensor Networks: an information processing approach”, Else vier publication, 2004.
6. C.S.Raghavendra Krishna, M.Sivalingam and Tarib znati, “Wireless Sensor Networks”, Springer publication, 2004.
7. Holger Karl , Andreas willig, “Protocol and Architecture for Wireless Sensor Networks”, John wiley publication, Jan 2006.
8. K.Akkaya and M.Younis, “ A Survey of routing protocols in wireless sensor networks”, Elsevier Adhoc Network Journal, Vol.3, no.3,pp. 325-349, 2005.
9. Philip Levis, “ TinyOS Programming”, 2006 – www.tinyos.net.
10. I.F. Akyildiz, W. Su, Sankarasubramaniam, E. Cayirci, “Wireless sensor networks: a survey”, computer networks, Elsevier, 2002, 394 - 422.
11. Jamal N. Al-karaki, Ahmed E. Kamal, “Routing Techniques in Wireless sensor networks: A survey”, IEEE wireless communication, December 2004, 6 – 28.