**PMA 15103 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS** **3 2 0 4**

**COURSEOBJECTIVES**

To enable the students to

- Gain fundamental knowledge of fuzzy sets, fuzzy logic, fuzzy decision making and fuzzy control systems.
- Focus on the concept to random variables and distributions.
- Understand the concepts of matrix theory
- Know about dynamic programming and its applications.
- Understand and compute quantitative metrics of performance for queuing systems.

**UNIT I FUZZY LOGIC** **9+6**

Classical logic–Multi valued logics–Fuzzy propositions–Fuzzy quantifiers

**UNIT II MATRIXTHEORY** **9+6**

Generalized Eigen values and Eigen vectors - Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications

**UNIT III ONE DIMENSIONAL RANDOM VARIABLES** **9+6**

Random variables-Probability function–moments–moment generating functions and their properties–Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions

**UNIT IV DYNAMIC PROGRAMMING** **9+6**

Dynamic programming – Principle of optimality – Forward and backward recursion –Applications of dynamic programming– Problem of dimensionality

**UNIT V QUEUING MODELS** **9+6**

Markovian queues – Single and Multi-server Models – Little's formula -Machine Interference Model – Steady State analysis– Self Service queue.

**TOTAL PERIODS 45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Understand the basic principles of fuzzy logic.
- Learn the basics and gained the skill for specialized studies and research.

- Develop efficient algorithms for solving dynamic programming problems, to acquire skills in Handling situation involving random variable.
- Know the basic characteristic features of a queuing system and acquire skills in analyzing Queuing models.

**TEXT BOOKS**


1.George J.KlirandYuan,B., "Fuzzy sets and fuzzy logic, Theory and applications," Prentice Hall of India Pvt. Ltd., 1997.

2.Moon,T.K.,Sterling,W.C.,"Mathematical methods and algorithms for signal processing", Pearson Education,2000.

3.Richard Johnson, Miller & Freund's, "Probability and Statistics for Engineers",7th Edition,Prentice Hall of India, Private Ltd., New Delhi (2007).

4.Taha,H.A.,"Operations Research, An introduction",7th edition, Pearson education editions, Asia, NewDelhi, 2002.

5.Donald Gross and Carl M.Harris, "Fundamentals of Queuing theory",2nd edition, John Wiley and Sons,NewYork(1985).


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | 3 | - | 3 | - | - | - | - | 3 | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 3 | 3 | - | 3 | - | - | - | - | 3 | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 | 3 | 3 |

**PVL 15102 DIGITAL SIGNAL PROCESSING INTEGRATED CIRCUITS** **3 2 0 4**

**COURSE OBJECTIVES**

To enable the students to

- familiarize the Number systems concept and Arithmetic Units.
- Understand the concepts of Digital signal processing.
- Study the concepts & gain knowledge about digital filters.
- Know the DSP architectures.
- Understand the Design of integrated circuit design.

**UNIT I NUMBER SYSTEMS AND ARITHMETIC UNITS** **9+6**

Conventional Number system, Redundant Number system, Residue Number System, Bit Parallel and Bit Serial Arithmetic, Distributed arithmetic, Basic Shift Accumulator, Reducing the memory size, Complex multipliers, improved shift-Accumulator.

**UNIT II DIGITAL SIGNAL PROCESSING** **9+6**

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT- The Discrete Fourier Transform, FFT- The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

**UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS** **9+6**

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, multi rate filters. Finite word length effects-Parasitic oscillations, Scaling of signal levels, Round- off noise, measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

**UNIT IV DSPINTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES** **9+6**

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated Circuits design.MOS transistors, MOS Logic, VLSI Process technologies Trends in CMOS technologies.

**UNIT V DSP ARCHITECTURES AND SYNTHESIS OF DSPARCHITECTURES** **9+6**

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multi-computers, Systolic and Wave front arrays, Shared memory architectures – Mapping of DSP algorithms on to hardware, Implementation based on complex PEs, Shared memory architecture with Bit–serial PEs.

**TOTAL PERIODS 45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Learn the basics of DSP processors.
- Learn the concepts of digital signal processing.
- Design different digital filters.
- Understand DSP architectures.
- Design the digital integrated circuits.

**TEXT BOOKS**


1. Lars Wan hammer, **"**DSP Integrated Circuits**"**, Academic press, New York1999.
2. A.V.Oppenheimet.al, "Discrete-time Signal Processing" Pearson education,2000.
3. Emmanuel C.I feachor, Barrie W.Jervis,**"**Digital signal processing – A practical approach**",** Second edition, Pearson education, Asia 2001.
4. Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation" John Wiley & Sons, 1999.
5. Bayoumi & Magdy A.,"VLSI Design Methodologies for Digital Signal Processing Architectures", BS Publications,2005.


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| **COs** | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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| **CO1** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO5** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15103 ADVANCED DIGITAL SYSTEM DESIGN** **3 2 0 4**

**COURSE OBJECTIVES**

To enable the students to

- familiarize the practical issues of sequential circuit design.
- Understand the concepts of Asynchronous Sequential Circuit Design.
- Study the concepts & gain knowledge about different fault diagnosis and testing methods.
- Know the concepts of programmable Devices.

**UNIT I SEQUENTIAL CIRCUIT DESIGN** **9+6**

Analysis of Clocked Synchronous Sequential Networks (CSSN)-Modeling of CSSN–State Assignment And Reduction–Design of CSSN–Design of Iterative Circuits–ASM Char t–ASM Realization, Design of Arithmetic circuits for Fast adder –Array Multiplier.

**UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN** **9+6**

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Design of Hazard free circuits - Data Synchronizers –Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits. Practical issues such as clocks kew, synchronous and asynchronous inputs and switch bouncing.

**UNIT III FAULT DIAGNOSIS & TESTING** **9+6**

Fault diagnosis: Fault Table Method – Path Sensitization Method – Boolean Difference Method –Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm. Design for testability: Test Generation – Masking Cycle–DFT Schemes. Circuit testing fault model, specific and random faults, testing of sequential circuits, Built in Self Test, Built in Logic Block observer(BILBO),signature analysis.

**UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES** **9+6**

EPROM to Realize a Sequential Circuit – Programmable Logic Devices Designing a Synchronous Sequential Circuit using a GAL–EPROM–Realization State machine using PLD–FPGA–Xilinx FPGA–Xilinx2000-Xilinx3000.

**UNIT V SYSTEM DESIGN USING VHDL** **9+6**

Design flow - VHDL Code Structure – Library, Entity, Architecture - Behavioural, Data flow and Structural modelling - Data Types - Operators and Attributes – Signals and Variables - Concurrent and Sequential Code–Packages and Components–Sub programs: Functions and Procedures–Design Examples-Test Benches.

**TOTAL PERIODS 45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Learn the synchronous sequential circuit design.
- Learn the design of Asynchronous sequential circuit design.
- Know about Fault Diagnosis & Testing Methods.
- Study the programmable logic devices.
- Carry out the system design using VHDL.

**REFERENCES**


1.Charles H.Roth Jr "Fundamentals of Logic Design", Thomson Learning2004.

2.ParagK.Lala "An introduction to Logic Circuit Testing" Morgan and clay pool publishers,2009.

3.J.F.Wakerly, "Digital Design principles and practices", PHI publications,2005.

4.Mark Zwolinski, "Digital System Design with VHDL" Pearson Education,2004.

5.H.Charles Roth, "Fundamentals of Logic design", Thoms on Learning,2003.


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| CO5 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |

**PVL15104** **VLSI DESIGN TECHNIQUES** **3 2 0 4**

**COURS EOBJECTIVES**

To enable the students to

- Study the basics of MOS transistor and IC fabrication.
- Learn in verters characteristics and logic function.
- Understand circuit characterization and performance estimation.
- familarise VLSI components circuits.
- Learn Verilog HDL and design VLSI circuits.

**UNITI VLSI DESIGN PROCESS AND MOS TRANSISTOR THEORY** **9+6**

VLSI Design Process – Architectural Design – Logical Design – Physical Design – Layout Styles –Full custom, Semi custom approaches. MOS transistors, CMOS logic, MOS transistor theory–Introduction, Enhancement mode transistor action, Ideal I-V characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model, Non ideal I-V effects, DC transfer characteristics, VLSI Design flow.

**UNIT II INVERTERS AND LOGIC GATES** **9+6**

NMOS and CMOS Inverters-Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures; Transmission gates- Static CMOS design, dynamic CMOS design.

**UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION** **9+6**

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining, Charge sharing, Scaling.

**UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS** **9+6**

Multiplexers, Decoders, comparators, priority encoders, Shift registers Arithmetic circuits–Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers.

**UNIT V VERILOG HARDWARE LANGUAGE** **9+6**

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

**TOTAL PERIODS** **45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Understand basics of MOS transistor and IC fabrication.
- Know inverters characteristics and logic function.

- Learn circuit characterization and performance estimation.
- Analyze the concepts of VLSI circuits.
- Understand Verilog HDL and design VLSI circuits.

**TEXTBOOKS**


1. Jan M Rabaey, “Digital Integrated Circuits”, Prentice Hall ofI ndia,2002.
2. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits-Analysis and Design Tata Mc Graw Hill,2003.
3. Neil H.E. Weste and Kamran Eshraghian, “Principles of CMO VLSI Design”, Pearson Education, ASIA, 2nd edition, 2000.
4. J.Bhasker,B.S.Publications, “A Verilog HDL Primer”,2nd Edition,2001.
5. Wayne Wolf “Modern VLSI Design Systemon chip”,Pearson Education,2002.


Mapping of Course Outcomes with Programme Outcomes:
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| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 |
| CO1 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO5 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15105 SOLID STATE DEVICE MODELING AND SIMULATION** **3 2 0 4**

**COURSE OBJECTIVES**

To enable the students to

- Know the basic semiconductor physics.
- Understand the basic concepts bipolar device modeling.
- know the operation of MOSFET modeling.
- Understand the Operation parameter measurement.
- Study the functions characteristics of opto electronic device modeling.

**UNIT I SEMICONDUCTO R PHYSICS** **9+6**

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity,Carrier Generation and Recombination, Avalanche Process, Noise Sources-Diodes : Forward and Reverse biased junctions – Reverse bias breakdown – Transient and AC conditions –Static and Dynamic behavior- Small and Large signal models – SPICE model for a Diode–Temperature and Area effects on Diode Model Parameters.

**UNIT II BIPOLAR DEVICE MODELING** **9+6**

Transistor Models: BJT–Transistor Action–Minority carrier distribution and Terminal currents-Switching-Eber-Molls and Gummel Poon Model, SPICE modeling-temperature and area effects.

**UNIT III MOSFET MODELING** **9+6**

OS Transistor –NMOS, PMOS–MOS Device equations-Threshold Voltage–Second order effects-Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

**UNIT IV PARAMETER MEASUREMENT** **9+6**

Bipolar Junction Transistor Parameter – Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques, Gummel Plots, MOSFET: Long and Short Channel Parameters, Measurement of Capacitance.

**UNIT V OPTO ELECTRONIC DEVICE MODELING** **9+6**

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

**TOTAL PERIODS 45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Know the fundamental of semiconductor physics.

- Understand BJTmodeling.
- Understand and design MOSFET modeling.
- Analyze opto electronic device modeling methods.

**TEXT BOOKS**


1.Ben.G.Streetman,"Solid State Devices" ,Prentice Hall,1997.

2.Giuseppe Masso brio and Paolo Anto gentti, "Semiconductor Device Modeling with SPICE", Second Edition,McGraw-HillInc,NewYork,1993.

3.Mohammed Ismail &Terri Fiez "Analog VLSI-Signal & Information Processing"1st edition,Tata Mc Graw Hill Publishing Company Ltd 2001.

4.Roulston E.J., "Bipolar Semiconductor Devices",Mc-GrawHill,1990.

5.Tor.A.Fijedly,"Introduction to Device Modelling and Circuit Simulation",Wiley-interscience,1997.


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL 15151 LOW POWER VLSI DESIGN** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- Know the sources of power consumption in CMOS circuits
- Understand the various power reduction techniques and the power estimation methods.
- Study the design concepts of low power circuits.

**UNIT I POWER DISSIPATION IN CMOS** **9**

Hierarchy of limits of power–Sources of power consumption–Physics of power dissipation in CMOSFET devices- Basic principle of low power design.

**UNIT II POWER OPTIMIZATION** **9**

Logical level power optimization– Circuit level low power design–Circuit techniques for reducing power consumption in adders and multipliers CMOS Circuits design styles, Adders, Multipliers.

**UNIT III DESIGN OF LOW POWER CMOS CIRCUITS** **9**

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories–Low power clock, Inter connect and layout design – Advanced techniques– Special techniques.

**UNIT IV POWER ESTIMATION** **9**

Power estimation techniques–Logic level power estimation–Simulation power analysis–Probabilistic power analysis- Random Logic signals – Probabilistic power analysis techniques

**UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER** **9**

Synthesis for low power –Behavioral level transforms –Software design for low power –Sources of software power Dissipation –Software Power Estimation–Software Power optimization

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Learn the basic concepts and principles of CMOS.
- Learn the Techniques of reducing power consumption.
- Understand advanced and special techniques for low power systems.
- Learn about the techniques involved in power estimation.
- Know about software design for low power.

**PVL15107** **VLSI DESIGN LABORATORY I** **0 0 4 2**

## COURSE OBJECTIVES

- To understand HDL and design circuits using it.
- To gain the ability to write the programs in VHDL and Verilog for modeling digital circuits
- To study and verify the combinational and sequential logic circuits with various levels of modeling and EDA Tools.
- To know importance of basic electronics involved in the design of MOS circuits.

## LIST OF EXPERIMENTS

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using Verilog.
3. Writing Test Benches Using Verilog / VHDL
4. Design and Implementation of ALU using FPGA.
5. Simulation of NMOS and CMOS circuits using SPICE.
6. Design of Static and Dynamic Logic Circuits
7. Modeling of MOSFET using C.
8. Implementation of FFT, Digital Filters.
9. Implementation of DSP algorithms using software package.
10. Implementation of MAC Unit using FPGA.

**TOTAL: 60 PERIODS**

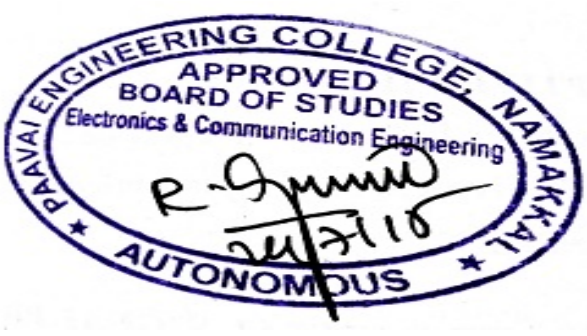
## COURSE OUTCOMES

At the end of this course, the students will be able to

- Make models of transistor circuits and simulate them for various operational requirements.
- Design the different types of multiplier using eda tool.
- Design the fir filter using eda tool.
- Analyze and design the VLSI circuits.

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |



**PVL15201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS** **3 2 0 4**

**COURSE OBJECTIVES**

To enable the students to

- Understand the operation of integrated circuits.
- analyze various devices in circuit configuration of integrated circuit.
- Impart in –depth knowledge about CMOS operational amplifier.
- Explore the concepts of PLL and its application.
- Learn fundamental concepts on ADC and DAC converters.

**UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES** **9+6**

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors –weak inversion in MOS transistors-substrate current flow in MOS transistor.

**UNIT II CIRCUIT CONFIGURATION FOR LINEARIC** **9+6**

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperatureindependent biasing techniques, voltage references - Output stages: Emitter follower, source follower and Push pullout put stages.

**UNIT III CMOS OPERATIONAL AMPLIFIERS** **9+6**

Buffered operational amplifiers- High speed and frequency operational amplifiers- Differential output operational Amplifiers –Microwave operational amplifiers-Low noise operational amplifiers- Low voltage operational amplifiers.

**UNIT IV ANALOG MULTIPLIER AND PLL** **9+6**

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise – Noise models of Integrated-circuit Components– Circuit Noise Calculations – Equivalent Input Noise Generators– Noise Band width–Noise Figure and Noise Temperature.

**UNIT V DIGITAL - ANALOG AND ANALOG- DIGITAL CONVERTERS** **9+6**

Introduction and characterization of DAC-Parallel DAC-Extending the resolution of parallel DAC-Serial DAC-Introduction and characterization of ADC-Serial ADC-Medium ADC-High speed ADC.

**TOTAL PERIODS** **45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Explain basic definitions and overview of CMOS integrated circuit.
- Acquire knowledge of how circuit configuration is made for Linear IC.
- Learn and analyze the problems in operational amplifier.
- Understand noise in analog amplifier circuit from a hierarchical view point.
- Apply advanced technical knowledge in MOS technology

**REFERENCES**


1.Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's",4thEdition,Wiley International,2002.

2.Behzad Razavi, "Design of Analog CMOS Integrated Circuits", S.Chand and company ltd,2000

3.Nandita Dasgupata, Amitava Dasgupta, "Semiconductor Devices, Modelling and Technology", Prentice Hall of India pvt.ltd, 2004.

4.Grebene, "Bipolar and MOS Analog Integrated circuit design",John Wiley& sons,Inc.,2003.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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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| **CO2** | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| **CO3** | 3 | 3 | - | - | - | 3 | - | - | - | - | 3 | 3 | 3 | 3 |
| **CO4** | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| **CO5** | 3 | 3 | - | - | - | 3 | - | - | - | - | 3 | 3 | 3 | 3 |

**PVL15202 COMPUTER AIDED DESIGN OF VLSI CIRCUITS** **3 2 0 4**

**COURSE OBJECTIVES**

To enable the students to

- Introduce the basic CAD algorithm.
- Understand the Partitioning.
- Study about Placement, Floor Planning
- Learn about Global, Detail routing
- Know the Modeling and synthesis in CAD flow.

**UNIT I LOGIC SYNTHESIS & BASIC ALGORITHMS** **9+6**

Introduction to combinational logic synthesis - Binary Decision Diagram - Hardware models for High-level synthesis-graph algorithms-computational geometry algorithms.

**UNIT II PARTITIONING** **9+6**

Classification of partitioning algorithms - Group migration algorithms - simulated annealing & evolution, other partitioning algorithms

**UNIT III PLACEMENT, FLOORPLANNING & PIN ASSIGNMENT** **9+6**

Simulation base placement algorithms, other placement algorithms-constraint based floor planning-floor planning algorithms for mixed block & cell design – General & channel pin assignment for register minimization

**UNIT IV ROUTING** **9+6**

Classification of global routing algorithms-Maze routing algorithm-line probe algorithm-Steiner Tree based algorithms – ILP based approaches-classification of routing algorithms-single layer routing algorithms, two layer Channel routing algorithms, three layer channel routing algorithms, and switch box routing algorithms.

**UNIT V MODELING AND SYNTHESIS** **9+6**

High level Synthesis-Hardware models – Internal representation - Allocation-assignment and scheduling–Simple scheduling algorithm – Assignment problem-High level transformations.

**TOTAL PERIODS** **45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Learn the Fundamentals of basic algorithm in CAD.
- Study the different partitioning algorithm.
- Understand the floor planning and placement algorithm.

- Learn about different routing algorithms.
- Know about modeling and synthesis techniques of CAD.

**REFERENCES**


1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das, "Networks-on-Chip "Architectures – A Holistic Design Exploration", Springer.

2.Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Inter connect",Morgan Kaufmann Publishers ©2008.

3.Frank Ghenassia, "Transaction Level Modeling with System C:TLM Concepts and Applications for Embedded Systems", Springer©2005(281pages),ISBN:9780387262321.

4.Luca Benini and Giovanni DeMicheli,"Networks on Chips: Technology and Tools", Morgan Kaufmann Publishers©2006(408pages),ISBN:9780123705211.

5.Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Chips theory and practice", CRCpress.


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 2 | - | - | 3 | - | - | 2 | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 2 | - | - | - | - | - | 2 | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 2 | - | - | 3 | - | - | 2 | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | - | - | - | - | - | 2 | - | - | 3 | 3 | 3 |
| **CO5** | 3 | 3 | 3 | - | - | 3 | - | - | 2 | - | - | 3 | 3 | 3 |

**PVL 15203 VLSI SIGNAL PROCESSING** **3 2 0 4**

**COURSE OBJECTIVES**

To enable the students to

- Understand the basic concepts of DSP algorithms.
- Know about the folding & unfolding concepts.
- Analyze the various pipelining and parallel processing techniques.
- Study the retiming and unfolding algorithms for various DSP applications.
- analyze the concept of various filters.

**UNIT I DSP SYSTEMS** **9+6**

Introduction to DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing–Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

**UNIT II RETIMING, FOLDING AND UNFOLDING** **9+6**

Retiming - definitions and properties Retiming techniques; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Folding – Folding transformation – Register minimizing techniques– Register minimization infolded architectures.

**UNIT III FAST CONVOLUTION** **9+6**

Fast convolution – Cook – Toom algorithm, modified Cook - Took algorithm – Iterated Convolution– Cyclic Convolution; Pipelined and parallel recursive and adaptive filters –inefficient /efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look – Ahead pipelining with power – of - twodecompositionparallelprocessingofIIRfilters,combinedpipeliningandparallelprocessingofIIRfilters, Pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

**UNIT IV BIT – LEVEL ARCHITECTURE AND SYSTOLI CARRAY DESIGN** **9+6**

Bit-Level Arithmetic Architectures – parallel multipliers with sign extension, parallel carry –ripple array multipliers, parallel carry – save multiplier, 4x4 bit Baugh- Wooley carry –save multiplication tabular form and implementation, design of Lyon's bit – serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement. Systolic array design methodology – FIR systolic Arrays–selection of scheduling vector-matrix multiplication and 2D systoli carray design-Systolic design for space Representations containing Delays.

**UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS** **9+6**

Synchronous, Wave and asynchronous pipelining – synchronous pipelining and clocking styles, clock skew in

edge-triggered single – phase clocking, two –phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design –needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

**TOTAL PERIODS 45+30**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Learn DSP algorithms.
- Understand and analyse the concept of pipelining and other processing for DSP applications
- Study about programming of digital signal processors.

**REFERENCES**


1. KeshabK.Parhi,"VLSIDigitalSignalProcessingsystems,Designandimplementation", Wiley,Inter Science,1999.
2. GaryYeap,"PracticalLowPowerDigitalVLSIDesign",KluwerAcademicPublishers,1998.
3. MohammedIsamailandTerriFiez,"AnalogVLSISignalandInformationProcessing",Mc Graw-Hill,1994.
4. JoseE.FranceandYannisTsividis,"DesignofAnalog-DigitalVLSICircuitsfor TelecommunicationandSignalProcessing",PrenticeHall,1994.
5. S.Y.Kung,H.J.WhiteHouse,T.Kailath,"VLSIandModernSignalProcessing",Prentice Hall,1985.


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 |
| CO1 | 3 | 3 | 3 | - | - | 3 | - | - | - | - | 3 | 3 | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | - | 3 | - | - | - | - | 3 | 3 | 3 | 3 |

**PVL 15251 CMOS VLSIDESIGN** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- Understand the basic CMOS circuits.
- Learn the CMOS process technology.
- Study the techniques of chip design using programmable devices.
- Learn the concepts of designing VLSI subsystems.
- Focus on the concepts of modeling a digital system using Hardware Description Language.

**UNIT I MOST RANSISTOR THEORY 9**

Introduction to I.C Technology- Basic MOS transistors –Threshold Voltage – Body effect – Basic D.C. Equations -Second order effects – MOS models – Small signal A.C characteristics – The complementary CMOS inverter-DC characteristics – Static Load MOS inverters – The differential inverters –Transmission gate.

**UNIT II CMOS PROCESSING TECHNOLOGY 9**

Silicon semiconductor technology - Wafer processing, Oxidation, epitaxy, deposition, Ion implantation – CMOS technology – n - well, p – well process – Silicon on insulator – CMOS process enhancement –Interconnect and circuit elements . Lay out design rules – Latch up.

**UNIT III CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION 9**

Resistance estimation - Capacitance estimation. MOS capacitor characteristics - Device capacitances – Diffusion capacitance Routing capacitance – Distributed RC effects – Inductance – Switching characteristics Rise time – Fall time. Delay time. Empirical delay models – Gate delays. CMOS gate transistorsizing –Power dissipation. Scaling of MOS transistor dimensions.

**UNIT IV CMOS CIRCUIT AND LOGIC DESIGN 9**

CMOS Logic gate design – Fan in and fan out. Typical CMOSN AND and NOR delays – Transistorsizing – CMOS logic structures - Complementary logic – BICM OS logic - Pseudo n MOS logic – Dynamic CMOS logic – Clocked CMOS logic – Pass transistor logic. CMOS domino logic. NP domino logic –Dual rail logic with suitable examples.

-Cascade voltages witch logic. Source follower pull up Logic (SFPL). Clocking strategies – I/O structures - Comparison of circuit families.

**UNIT V CMOS SUB SYSTEM DESIGN 9**

Data path operations - Addition/subtraction – Parity generators – Comparators – Zero/one detectors –Binary Counters - ALUs, Design of multipliers: Parallel Multipliers, Array, 2’s Complement, Booth – Braun – Baugh -

Wooley – Wallace tree, Dadda Multipliers, Serial Multiplication – Shifters – Memory elements - RWM, ROM, Content Addressable Memory .Control: FSM, PLA Control Implementation.

**TOTAL PERIODS 45**

**COURSE OUT COMES**

At the end of the course, the students will be able to

- Differentiate the ideal and non-ideal characteristics of MOSFET.
- Know various methodologies to fabricate an IC.
- Understand the switching characteristics and power reduction techniques.
- Know the circuit families.
- Design and analyze different CMOS subsystems.

**REFERENCES**


1. Neil. H.E. Weste and K. Eshragian, "Principles of CMOS VLSI Design", 2nd Edition. Addison - Wesley, 2000
2. Douglasa. Pucknell and K. Eshragian., "Basic VLSI Design" 3rdEdition.PHI, 2000
3. R. Jacob Baker, Harry W. LI., & David K. Boyce, "CMOS Circuit Design" , 3rd Indian reprint, PHI, 2000
4. N. Weste and D. Harris, "Introduction to CMOS VLSI design", Addision -, 3rd Edition, 2004.


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 |
| CO1 | 3 | 3 | 3 | - | - | 3 | - | - | - | - | - | 3 | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | - | 3 | - | - | - | - | - | 3 | 3 | 3 |
| CO4 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO5 | 3 | 3 | 3 | - | - | 3 | - | - | - | - | - | 3 | 3 | 3 |

**PVL 15351 ANALOG VLSI DESIGN** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the student to

- Acquire basic knowledge about CMOS circuit techniques and amplifier design
- Study about BICMOS circuits and signal processing
- Understand the concept behind A/D Converters and analog sensors
- Introduce the concept to testing of Analog VLSI circuits
- gatherknowledgeaboutstatisticalmodelingandsimulationofanalogcircuits

**UNIT I CMOS CIRCUIT TECHNIQUES , CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING** **9**

Mixed-Signal VLSI Chips- Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage Bi CMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

**UNIT II BI CMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING** **9**

Continuous- Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low- Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

**UNIT III ANALOG CMOS SUB CIRCUITS** **9**

CMOS Amplifiers MOS switch-MOS diode and active resistor-Current sinks and sources-Current mirrors-Current and voltage References:-Band gap References:-Invertors-Differential amplifiers-Cascode amplifiers–Current amplifiers-Output amplifiers-High gain amplifiers architectures.

**UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS** **9**

Fault modeling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan- Built- in Self Test-Analog Test Buses-Design for Electron-Beam Test ability-Physics of Interconnects in VLSI- Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Proto typing Analog Circuits.

**UNIT V DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS** **9**

Introduction and characterization of DAC-Parallel DAC-Extending there solution of parallel DAC-Serial DAC-Introduction and characterization of ADC-Serial ADC-Medium ADC- High speed ADC.

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course ,the students will be able to

- Learn the CMOS circuit design and low voltage signal processing
- Understand the basic BICMOS circuit techniques and models.
- Know about sampled data analog filters and A/D Converters
- Perform the statistical modeling and simulate the analog circuits

**REFERENCES**


1. Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing" ,McGraw-Hill InternationalEditons,1994.
2. MalcomR.Haskard,LanC.May,"AnalogVLSIDesign-NMOSandCMOS",PrenticeHall,1998.
3. RandallLGeiger,PhillipE.Allen,NoelK.Strader,"VLSI Design Techniques for Analog and digital Circuits",Mc GrawHill InternationalCompany,1990.
4. JoseE.France,YannisTsividis,"DesignofAnalog-DigitalVLSICircuitsfor Tele communication and Signal Processing",PrenticeHall,1994.


Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 |
| CO1 | 3 | 3 | 3 | 3 | - | 3 | - | - | - | - | - | 3 | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | - | 3 | - | - | - | - | - | 3 | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL 15454 VLSI FOR WIRELESS COMMUNICATION** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- Understand the basics of wireless communication.
- Understand the concepts of transceiver architectures.
- Introduce to the students the low power design techniques of VLSI circuits.
- Learn the design and implementation of various VLSI circuits for wireless communication systems.

**UNIT I WIRELESS COMMUNICATION** **9**

Digital communication systems- minimum bandwidth requirement, the Shan on limit- overview of modulation schemes- classical channel- wireless channel description- path loss- multipath fading- basics of spread spectrum and spread spectrum techniques-PN sequence.

**UNIT II TRANSCEIVER ARCHITECTURE** **9**

Transceiver design constraints-base band subsystem design-RF sub system design-Super heterodyne receiver and direct conversion receiver- Receiver front-end- filter design- non-idealities and design parameters- derivation of noise figure and IP3 of receiver front end.

**UNIT III LOW POWER DESIGN TECHNIQUES** **9**

Source of power dissipation-estimation of power dissipation-reducing power dissipation at device and circuit levels-low voltage and low power operation- reducing power dissipation at architecture and algorithm levels.

**UNIT IV WIRELESS CIRCUITS** **9**

VLSI Design of LNA- wide band and narrow band- impedance matching- Automatic Gain Control(AGC)amplifier power amplifier- Active mixer- analysis, conversion gain, distortion analysis- low frequency and high frequency case, noise- Passive mixer- sampling mixer and switching mixer-analysis of distortion, conversion gain and noise

In these mixers.

**UNIT V VLSI DESIGN OF SYNTHESIZERS** **9**

VLSI design of Frequency Synthesizers(FS)–Parameters of FS-PLL based frequency synthesizer, phase detector/ charge pump-dividers-VCO-LC oscillators- ring oscillator-phase noise-loop filter-description, design approaches.

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- Understand the application of VLSI circuits in wireless communication.
- Gain knowledge of various architectures used in implementing wire less systems.
- Know about design and simulation of low power techniques using software
- Learn the VLSI design of wireless circuits.

**REFERENCES**


1. Bos co Leung,“ VLSI for WirelessCommunication”,Springer,2011.
2. Elmad N Fara gand Mohamed IEl masry, “Mixed Signal VLSI Wireless Design-Circuits and Systems”, Kluwer Academic Publishers,2002.


| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | - | - | 3 | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 3 | - | - | 3 | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15204** **VLSI DESIGN LAB II** **0 0 4 2**

**COURSE OBJECTIVES**

- To implement 8 Bit ALU in FPGA / CPLD
- To implement 4 Bit Sliced processor in FPGA / CPLD
- To implement elevator controller using embedded microcontroller
- To implement alarm clock controller using embedded microcontroller
- To implement model train controller using embedded microcontroller
- To implement the system design using PLL

**LIST OF EXPERIMENTS**

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD
3. Implementation of Elevator controller using embedded microcontroller.
4. Implementation of Alarm clock controller using embedded microcontroller.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.
7. Design and simulation of circuits for gate level event driven simulation.
8. Design and simulation of BIST architectures
9. Design of Minimum Spanning Tree and Partitioning Algorithm.
10. Mini Project

**TOTAL: 60 PERIODS**

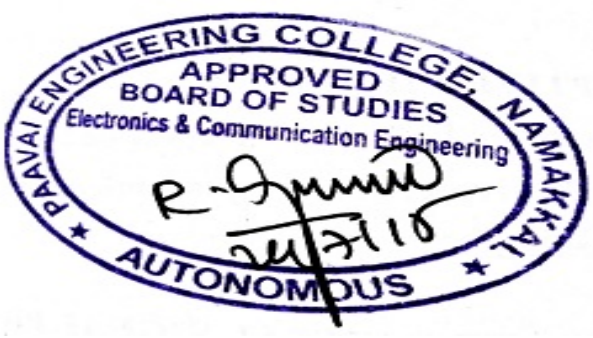
**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Write HDL code for basic as well as advanced digital integrated circuits.
- Import the logic modules into FPGA boards.
- Synthesize place and route the digital ICS.
- Design, Simulate and Extract the layouts of Analog IC Blocks using EDA tools.

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |



**VL7211** **VLSI DESIGN LABORATORY II** **L T P C**
**0 0 3 2**

1. Design and simulate frequency response and noise analysis of any Source followers
2. Design and simulate Design and simulate operational amplifier performance parameters - One-stage Op Amps, Two-stage Op Amps
3. Design and simulate cascode current mirrors and active current mirrors
4. Design of various routing - local routing, Area routing, channel routing and global routing
5. Design and Simulation of Gate-level modeling
6. Design and Simulation of Switch-level modeling
7. Modeling and synthesis of simple scheduling algorithm
8. Design and implement reducing power consumption in memories
9. Design and simulate Power Estimation

**TOTAL: 45 PERIODS**

**VL7301** **TESTING OF VLSI CIRCUITS** **L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To know the various types of faults and also to study about fault detection, dominance
- To know the concepts of the test generation methods-DFT-BIST.
- To understand the fault diagnosis methods.

**UNIT I TESTING AND FAULT MODELLING** **9**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

**UNIT II TEST GENERATION** **9**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

**UNIT III DESIGN FOR TESTABILITY** **9**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

**UNIT IV SELF – TEST AND TEST ALGORITHMS** **9**

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

**UNIT V FAULT DIAGNOSIS** **9**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

**VL7211 VLSI DESIGN LABORATORY II L T P C**
**0 0 3 2**

1. Design and simulate frequency response and noise analysis of any Source followers
2. Design and simulate Design and simulate operational amplifier performance parameters - One-stage Op Amps, Two-stage Op Amps
3. Design and simulate cascode current mirrors and active current mirrors
4. Design of various routing - local routing, Area routing, channel routing and global routing
5. Design and Simulation of Gate-level modeling
6. Design and Simulation of Switch-level modeling
7. Modeling and synthesis of simple scheduling algorithm
8. Design and implement reducing power consumption in memories
9. Design and simulate Power Estimation

**TOTAL: 45 PERIODS**

**VL7301 TESTING OF VLSI CIRCUITS L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To know the various types of faults and also to study about fault detection, dominance
- To know the concepts of the test generation methods-DFT-BIST.
- To understand the fault diagnosis methods.

**UNIT I TESTING AND FAULT MODELLING 9**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

**UNIT II TEST GENERATION 9**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

**UNIT III DESIGN FOR TESTABILITY 9**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

**UNIT IV SELF – TEST AND TEST ALGORITHMS 9**

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

**UNIT V FAULT DIAGNOSIS 9**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

**TOTAL: 45 PERIODS**

**REFERENCES:**


1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

**AP7010 DATA CONVERTERS L T P C**
**3 0 0 3**

**OBJECTIVE:**

- To study the A/D and D/A architectures
  To study the importance of sample and hold circuits in A/D and D/A conversion techniques.

**UNIT I SAMPLE AND HOLD CIRCUITS 9**

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

**UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9**

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

**UNIT III DIGITAL TO ANALOG CONVERSION 9**

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

**UNIT IV ANALOG TO DIGITAL CONVERSION 9**

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

**UNIT V PRECISION TECHNIQUES 9**

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

**TOTAL:45 PERIODS**

**REFERENCE:**

1. Behzad Razavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

**VL7013 VLSI FOR WIRELESS COMMUNICATION L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication.

**UNIT I COMPONENTS AND DEVICES 9**

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

**UNIT II MIXERS 9**

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise - A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

**UNIT III FREQUENCY SYNTHESIZERS 9**

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

**UNIT IV UB SYSTEMS 9**

Data converters in communications, adaptive Filters, equalizers and transceivers

**UNIT V IMPLEMENTATIONS 9**

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System .

**TOTAL:45 PERIODS**

**REFERENCES:**


1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.
4. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2000.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
6. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.


**VL7014 IP BASED VLSI DESIGN L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To learn about IC manufacturing and fabrication
- To analyse the combinational, sequential and subsystem design
- To study about different floor planning techniques and architecture design
- To have an introduction to IP design security

**UNIT I VLSI AND ITS FABRICATION 9**

Introduction, IC manufacturing, CMOS technology, IC design techniques, IP based design, Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability, Layout Design and tools.

**UNIT II COMBINATIONAL LOGIC NETWORKS 9**

Logic Gates: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Delay, Yield, Gates as IP, Combinational Logic Networks-Standard Cell based Layout, Combinational network delay, Logic and Interconnect design, Power optimization, Switch logic network, logic testing;

**UNIT III SUBSYSTEM DESIGN 9**

Sequential Machine-Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing; Subsystem Design-Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors, FPGA,PLA, Buses and NoC, Data paths, Subsystems as IP.

**UNIT IV FLOOR PLANNING AND ARCHITECTURE DESIGN 9**

Floor planning-Floor planning methods, Global Interconnect, Floor plan design, Off-chip Connections Architecture Design- HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP Components, Design Methodologies, Multiprocessor System-on-chip Design

**UNIT V DESIGN SECURITY 9**

IP in reuse based design, Constrained based IP protection, Protection of data and Privacy-constrained based watermarking for VLSI IP based protection

**TOTAL:45 PERIODS**

**REFERENCES:**

1. Wayne wolf, “Modern VLSI Design:IP-based Design”, Pearson Education,2009.
2. Qu gang, Miodrag potkonjak, “Intellectual Property Protection in VLSI Designs: Theory and Practice”, kluwer academic publishers,2003.

**VL7015 NANOSCALE DEVICES AND CIRCUIT DESIGN L T P C**
**3 0 0 3**

**OBJECTIVES:**

1. To learn about leakage current and its control and reduction techniques in CMOS devices.
2. To know the device technologies for sub 100nm CMOS.
3. To study the device scaling of single and multigate MOSFETs.
4. To familiarize the low power design and voltage scaling issues in Nano scale devices.
5. To study about various nanoscale devices.
6. To design CMOS circuit using non-classical devices**.**

**UNIT I CMOS SCALING CHALLENGES IN NANOSCALE REGIMES 9**

Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, process variations in devices and interconnects. **Device technologies for sub 100nm CMOS:** Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate; Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs.

**UNIT II DEVICE SCALING AND BALLISTIC MOSFET 9**

Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in MOSFTEs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs.

**UNIT III EMERGING NANOSCALE DEVICES 9**

Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices.

**UNIT IV NANOSCALE CMOS DESIGN 9**

CMOS logic power and performance, voltage scaling issues; Introduction to low power design; Performance optimization for data paths.

**UNIT V NANOSCALE CIRCUITS 9**

Statistical circuit design, variability reduction, design for manufacturing and design optimization; Sequential logic circuits, registers, timing and clock distribution, IO circuits and memory design and trends. **Non-classical CMOS**: CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

**TOTAL : 45 PERIODS**

**REFERENCES:**

1. Lundstrom, M., “Nanoscale Transport: Device Physics, Modeling, and Simulation”, Springer. 2000
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., “Strained-Si and Hetrostructure Field Effect Devices”, Taylor and Francis, 2007
3. Hanson, G.W., “Fundamentals of Nanoelectronics”, Pearson, India., 2008.
4. Wong, B.P., Mittal, A., Cao Y. and Starr, G., “Nano-CMOS Circuit and Physical Design”, Wiley, 2004
5. Lavagno, L., Scheffer, L. and Martin, G., “EDA for IC Implementation Circuit Design and Process Technology”, Taylor and Francis, 2005

**REFERENCES:**


1. Deep-Submicron Cmos Ics: From Basics to Asics By Harry J. M. Veendrick
2. Low Power Design in Deep Submicron Electronics by W. Nebel, Jean P. Mermet
3. Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction by P.R. Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund


**AP7301 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To understand the basics of EMI
- To study EMI Sources
- To understand EMI problems
- To understand Solution methods in PCB
- To understand Measurement technique for emission
- To understand Measurement technique for immunity

**UNIT I EMI/EMC CONCEPTS 9**

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

**UNIT II EMI COUPLING PRINCIPLES 9**

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

**UNIT III EMI CONTROL TECHNIQUES 9**

Shielding- Shielding Material-Shielding integrity at discontinuties, Filtering- Characteristics of Filters-Impedance and Lumped element filters-Telephone line filter, Power line filter design, Filter installation and Evaluation, Grounding- Measurement of Ground resistance-system grounding for EMI/EMC-Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control. EMI gaskets

**UNIT IV EMC DESIGN OF PCBS 9**

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits ,Component selection and mounting; PCB trace impedance; Routing; Cross talk control-Electromagnetic Pulse-Noise from relays and switches, Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

**UNIT V EMI MEASUREMENTS AND STANDARDS 9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Frequency assignment - spectrum conversation. British VDE standards, Euro norms standards in japan - comparisons. EN Emission and Susceptibility standards and Specifications.

**TOTAL: 45PERIODS**

**OUTCOMES**

Upon Completion of the course, the students will be able to

- To design a EMI free system
- To reduce system level crosstalk
- To design high speed Printed Circuit board with minimum interference
- To make our world free from unwanted electromagnetic environment

**REFERENCES:**


1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, New York, 1996.
2. Clayton R.Paul,” Introduction to Electromagnetic Compatibility”, John Wiley Publications, 2008
3. Henry W.Ott., ”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science
4. Publications, John Wiley and Sons, Newyork, 1988.
5. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Don R.J. White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.


| VL7011 | SIGNAL INTEGRITY FOR HIGH SPEED DEVICES | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |

**OBJECTIVES:**

1. To learn the fundamental and importance of signal integrity.
2. To analyze and minimize cross talk in unbounded conductive media.
3. To study about the different types of Di-Electric materials.
4. To learn about differential cross talk and CMOS based transmission line model

**UNIT I FUNDAMENTALS 9**

The importance of signal integrity-new realm of bus design-Electromagnetic fundamentals for signal integrity-maxwell equations common vector operators-wave propagations-Electrostatics-magneto statics-Power flow and the poynting vector-Reflections of electromagnetic waves

**UNIT II CROSS TALK 9**

Introduction -mutual inductance and capacitance-coupled wave equation-coupled line analysis-modal analysis-cross talk minimization signal propagation in unbounded conductive media-classic conductor model for transmission model

**UNIT III DI-ELECTRIC MATERIALS 9**

Polarization of Dielectric-Classification of Di electric material-frequency dependent di electric material- Classification of Di electric material fiber-Weave effect-Environmental variation in di electric behaviour Transmission line parameters for loosy dielectric and realistics conductors

**UNIT IV DIFFERENTIAL SIGNALING 9**

Removal of common mode noise-Differential Cross talk-Virtual reference plane-propagation of model voltages common terminology-drawbacks of Differential signaling

**UNIT V PHYSICAL TRANSMISSION LINE MODEL 9**

Introduction- non ideal return paths-Vias-IO design consideration-Push-pull transmitter-CMOS receivers-ESSD protection circuits-On chip Termination

**TOTAL:45 PERIODS**

**REFERENCES:**


1. Advanced Signal Integrity for High-Speed Digital Designs By Stephen H. Hall, Howard L. Heck
2. Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS by James Edgar Buchanan

**VL7012 MIXED SIGNAL IC TEST AND MEASUREMENTS L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To know about mixed-signal devices and the need for testing these devices.
- To study the various techniques for testing.
- To learn about DSP based testing.
- To understand the benefits and techniques of DFT.
- To study the general purpose measuring devices.

**UNIT I OVERVIEW OF MIXED – SIGNAL TESTING 9**

MIXED – SIGNAL CIRCUITS Common Types of Analog and Mixed- Signal Circuits – Applications of Mixed-Signal Circuits - The CMOS Fabrication process – Real –World Circuits – What Is a Test Engineer Post Silicon Production Flow-Test and Packing – Characterization versus Production Testing Test and Diagnostic Equipments-Automated Test Equipments – Wafer Probers – Handlers – E-Beam Probers – Focused Ion Beam Equipments – Forced -Temperature

**UNIT II DC AND PARAMETRIC MEASUREMENT 9**

Purpose of Continuity Testing – Continuity Test Techniques – Serial Versus Parallel Continuity Testing Purpose of Leakage Testing – Leakage Test Technique – Serial versus Parallel Leakage Testing Importance of Supply current tests – Test Techniques Voltage Regulators – Voltage References – Trimmable References Input Impedance – Output Impedance – Differential Impedance Measurements $V_{MID}$ and Analog Ground - DC transfer Characteristics (Gain and Offset) – Output Offset Voltage (Vo) – Single-Ended, Differential and Common-Model Offsets – Input Offset Voltage (Vos) Closed-Loop Gain – Open – Loop Gain DC power supply sensitivity – DC Power Supply Rejection Ration

**UNIT III TESTER HARDWARE 9**

General-Purpose Tester versus Focused Bench Equipment – Generic Tester Architecture General-Purpose Multimeters – General-Purpose Voltage/Current Sources – Precision Voltage References and User Supplies – Calibration Source – Relay Matrices – Relay Control Lines Digital Vectors – Digital Signals – Source Memory – Capture Memory - Pin Card Electronics – Timing and Formatting Electronics AC Continuous Wave source and AC Meter – Arbitrary Waveform Generators- Waveform Digitizers – Clocking and Synchronization Time Measurements – Time Measurement Interconnects

**UNIT IV DSP – BASED TESTING 9**

Reduced Test Time – Separation of Signal Components – Advanced Signal Manipulations DSP and Array Processing – Fourier Analysis of Periodic Signals – The Trigonometric Fourier Series – The Discrete- Time Fourier Series – Complete Frequency Renormalization The Discrete Fourier Transform – The Fast Fourier Transform – Interpreting the FFT Output Equivalence of Time- and Frequency – Domain Information – Parseval's Theorem – Applications of the Inverse FFT – Frequency – Domain Filtering – Noise Weighting

**UNIT V DESIGN FOR TEST (DFT) 9**

Built- In Self-Test – Differences between Digital Dft and Analog Dft Lower Cost of Test – Increased Fault Coverage and Improved Process Control – Diagnostics and Characterization – Diagnostics and Characterization – Ease of Test Program Development- System- Level Diagnostics – Economics of DfT Scan Basics – IEEE Std. 1149. 1 Standard Test Access Port and Boundary Scan – Full Scan and Partial Scan Pseudorandom BILBO Circuits – Memory BIST – Microcode BIST Partitioning – Digital Resets and Presets – Device-Driven Timing – Lengthy Preambles Mixed – Signal Boundary Scan (IEEE Std. 1149.4) - Analog and Mixed-Signal BIST

**TOTAL:45 PERIODS**

**REFERENCES:**


1. An Introduction to Mixed-signal IC Test and Measurement by Gordon W.Roberts, Friedrich Taenzler, Mark Burns
2. Analog and mixed-signal test by Bapiraju Vinnakota
3. Digital and Analogue Instrumentation: Testing and Measurement by Nihal Kularatna

**AP7010** **DATA CONVERTERS** **L T P C**
**3 0 0 3**

**OBJECTIVE:**

- To study the A/D and D/A architectures
  To study the importance of sample and hold circuits in A/D and D/A conversion techniques.

**UNIT I SAMPLE AND HOLD CIRCUITS 9**

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

**UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9**

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

**UNIT III DIGITAL TO ANALOG CONVERSION 9**

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

**UNIT IV ANALOG TO DIGITAL CONVERSION 9**

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

**UNIT V PRECISION TECHNIQUES 9**

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

**TOTAL:45 PERIODS**

**REFERENCE:**

1. Behzad Razavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

**VL7013** **VLSI FOR WIRELESS COMMUNICATION** **L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication.

**UNIT I COMPONENTS AND DEVICES 9**

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

**UNIT II MIXERS 9**

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise - A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

**UNIT III FREQUENCY SYNTHESIZERS 9**

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

**UNIT IV UB SYSTEMS 9**

Data converters in communications, adaptive Filters, equalizers and transceivers

**UNIT V IMPLEMENTATIONS 9**

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System .

**TOTAL:45 PERIODS**

**REFERENCES:**


1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.
4. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2000.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
6. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.


**VL7014 IP BASED VLSI DESIGN L T P C**
**3 0 0 3**

**OBJECTIVES:**

- To learn about IC manufacturing and fabrication
- To analyse the combinational, sequential and subsystem design
- To study about different floor planning techniques and architecture design
- To have an introduction to IP design security

**UNIT I VLSI AND ITS FABRICATION 9**

Introduction, IC manufacturing, CMOS technology, IC design techniques, IP based design, Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability, Layout Design and tools.

**UNIT II COMBINATIONAL LOGIC NETWORKS 9**

Logic Gates: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Delay, Yield, Gates as IP, Combinational Logic Networks-Standard Cell based Layout, Combinational network delay, Logic and Interconnect design, Power optimization, Switch logic network, logic testing;

**UNIT III SUBSYSTEM DESIGN 9**

Sequential Machine-Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing; Subsystem Design-Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors, FPGA,PLA, Buses and NoC, Data paths, Subsystems as IP.

**UNIT IV FLOOR PLANNING AND ARCHITECTURE DESIGN 9**

Floor planning-Floor planning methods, Global Interconnect, Floor plan design, Off-chip Connections Architecture Design- HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP Components, Design Methodologies, Multiprocessor System-on-chip Design

**UNIT V DESIGN SECURITY 9**

IP in reuse based design, Constrained based IP protection, Protection of data and Privacy-constrained based watermarking for VLSI IP based protection

**TOTAL:45 PERIODS**

**REFERENCES:**


1. Wayne wolf, "Modern VLSI Design:IP-based Design", Pearson Education,2009.
2. Qu gang, Miodrag potkonjak, "Intellectual Property Protection in VLSI Designs: Theory and Practice", kluwer academic publishers,2003.


**VL7015 NANOSCALE DEVICES AND CIRCUIT DESIGN L T P C**
**3 0 0 3**

**OBJECTIVES:**

1. To learn about leakage current and its control and reduction techniques in CMOS devices.
2. To know the device technologies for sub 100nm CMOS.
3. To study the device scaling of single and multigate MOSFETs.
4. To familiarize the low power design and voltage scaling issues in Nano scale devices.
5. To study about various nanoscale devices.
6. To design CMOS circuit using non-classical devices**.**

**UNIT I CMOS SCALING CHALLENGES IN NANOSCALE REGIMES 9**

Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, process variations in devices and interconnects. **Device technologies for sub 100nm CMOS:** Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate; Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs.

**UNIT II DEVICE SCALING AND BALLISTIC MOSFET 9**

Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in MOSFTEs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs.

**UNIT III EMERGING NANOSCALE DEVICES 9**

Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices.

**UNIT IV NANOSCALE CMOS DESIGN 9**

CMOS logic power and performance, voltage scaling issues; Introduction to low power design; Performance optimization for data paths.

**UNIT V NANOSCALE CIRCUITS 9**

Statistical circuit design, variability reduction, design for manufacturing and design optimization; Sequential logic circuits, registers, timing and clock distribution, IO circuits and memory design and trends. **Non-classical CMOS**: CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

**TOTAL : 45 PERIODS**

**REFERENCES:**


1. Lundstrom, M., "Nanoscale Transport: Device Physics, Modeling, and Simulation", Springer. 2000
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., "Strained-Si and Hetrostructure Field Effect Devices", Taylor and Francis, 2007
3. Hanson, G.W., "Fundamentals of Nanoelectronics", Pearson, India., 2008.
4. Wong, B.P., Mittal, A., Cao Y. and Starr, G., "Nano-CMOS Circuit and Physical Design", Wiley, 2004
5. Lavagno, L., Scheffer, L. and Martin, G., "EDA for IC Implementation Circuit Design and Process Technology", Taylor and Francis, 2005