**SEMESTER I**

**PMA16103 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS 3 2 0 4**

**COURSE OBJECTIVES**

- To gain fundamental knowledge of fuzzy sets, fuzzy logic, fuzzy decision making and fuzzy control systems.
- To focus on the concept of ordinary differential equations.
- To understand the concepts of matrix theory
- To know about dynamic programming and its applications.
- To understand and compute quantitative metrics of performance for queuing systems.

**UNIT I FUZZY LOGIC 15**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers

**UNIT II MATRIX THEORY 15**

Generalized Eigen values and Eigen vectors - Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications

**UNIT III ORDINARY DIFFERENTIAL EQUATIONS 15**

Runge - Kutta Methods for system of IVPs – Numerical stability – Adams-Bashforth multistep method – Solution of stiff ODEs – shooting method – BVP: Finite difference method, orthogonal collocation method, orthogonal collocation with finite element method, Galerkin finite element method.

**UNIT IV DYNAMIC PROGRAMMING 15**

Dynamic programming – Principle of optimality – Forward and backward recursion –Applications of dynamic programming – Problem of dimensionality

**UNIT V QUEUING MODELS 15**

Markovian queues – Single and Multi-server Models – Little's formula -Machine Interference Model – Steady State analysis – Self Service queue.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Understand the basic principles of fuzzy logic.
- Know the basics and gained the skill for specialized studies and research.
- Develop efficient algorithms for solving dynamic programming problems, to acquire skills in handling situation involving random variable.
- Gain knowledge in the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.

**REFERENCES**

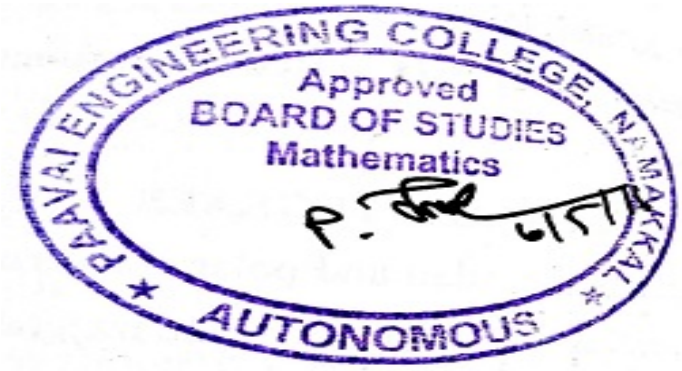

1. George J. Klir and Yuan, B., "Fuzzy sets and fuzzy logic, Theory and applications," Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., "Mathematical methods and algorithms for signal processing", Pearson Education, 2000.
3. Saumyen Guha and Rajesh Srivastava, "Numerical methods for Engineering and Science", Oxford Higher Education, New Delhi, 2010.
4. Taha, H.A., "Operations Research, An introduction", 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, "Fundamentals of Queuing theory", 2nd edition, John Wiley and Sons, New York (1985).


**WEB LINKS**

- https://www.youtube.com/watch?v=P8wY6mi1vV8
- https://www.youtube.com/watch?v=35UmpC6nrg8
- https://www.youtube.com/watch?v=RI1Ey1LkpxQ
- https://www.youtube.com/watch?v=c2DymN34w04

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |



**PVL16101 DIGITAL SIGNAL PROCESSING INTEGRATED CIRCUITS 3 2 0 4**

**COURSE OBJECTIVES**

- To familiarize the concept of number systems and arithmetic units.
- To understand the concepts of digital signal processing.
- To study the concepts and gain knowledge about digital filters.
- To know the DSP architectures.
- To understand the Design of integrated circuit design.

**UNIT I NUMBER SYSTEMS AND ARITHMETIC UNITS 15**

Conventional Number system, Redundant Number system, Residue Number System, Bit Parallel and Bit Serial Arithmetic, Distributed arithmetic, Basic Shift Accumulator, Reducing the memory size, Complex multipliers, improved shift-Accumulator.

**UNIT II DIGITAL SIGNAL PROCESSING 15**

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processingsystems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

**UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 15**

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, measuring round-off noise, Coefficient sensitivity, Sensitivity and noise

**UNIT I V DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 15**

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated Circuits design. MOS transistors, MOS Logic, VLSI Process technologies Trends in CMOS technologies

**UNIT V DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 15**

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multi-computers, Systolic and Wave front arrays, Shared memory architectures - Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the basics of DSP processors.
- Understand the concepts of digital signal processing.

- Design different digital filters.
- Understand DSP architectures.
- Design the digital integrated circuits.

**REFERENCES**


1. Lars Wanhammer, **"**DSP Integrated Circuits**"**, Academic press, New York 1999.
2. A.V.Oppenheim et.al, "Discrete-time Signal Processing" Pearson education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, **"**Digital signal processing – A practical approach**",** Second edition, Pearson education, Asia 2001.
4. Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation" John Wiley& Sons, 1999.
5. Bayoumi & Magdy A., "VLSI Design Methodologies for Digital Signal Processing Architectures", BS Publications, 2005.


**WEB LINKS**

1. http://nptel.ac.in/courses/117105075/
2. http://nptel.ac.in/courses/117101001/
3. https://www.youtube.com/watch?v=_hKArr0D8M8

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16102 ADVANCED DIGITAL SYSTEM DESIGN 3 2 0 4**

**COURSE OBJECTIVES**

- To familiarize the practical issues of sequential circuit design
- To understand the concepts of asynchronous sequential circuit design.
- To study the concepts and gain knowledge about different fault diagnosis and testing methods.
- To know the concepts of programmable devices.

**UNIT I SEQUENTIAL CIRCUIT DESIGN 15**

Analysis of Clocked Synchronous Sequential Networks (CSSN) - Modeling of CSSN –State Assignment and Reduction – Design of CSSN – Design of Iterative Circuits– ASM Chart – ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier

**UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 15**

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Design of Hazard free circuits - Data Synchronizers –Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits. Practical issues such as clock skew, synchronous and asynchronous inputs and switch bouncing

**UNIT III FAULT DIAGNOSIS & TESTING 15**

Fault diagnosis: Fault Table Method – Path Sensitization Method – Boolean Difference Method –Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm. Design for testability: Test Generation – Masking Cycle – DFT Schemes. Circuit testing fault model, specific and random faults, testing of sequential circuits, Built in Self Test, Built in Logic Block observer (BILBO), signature analysis.

**UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 15**

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA– Xilinx 2000 - Xilinx 3000

**UNIT V SYSTEM DESIGN USING VHDL 15**

Design flow - VHDL Code Structure – Library, Entity, Architecture - Behavioural, Data flow and Structural modelling - Data Types - Operators and Attributes – Signals and Variables - Concurrent and Sequential Code – Packages and Components – Subprograms: Functions and Procedures – Design Examples - Test Benches.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the synchronous sequential circuit design
- Design of asynchronous sequential circuit

- Know about fault diagnosis and testing methods
- Study the programmable logic devices
- Carry out the system design using VHDL

**REFERENCES**


1. Charles H.Roth Jr “Fundamentals of Logic Design”, Thomson Learning 2004.
2. Parag K.Lala “An introduction to Logic Circuit Testing” Morgan and clay pool publishers, 2009.
3. J.F.Wakerly, “Digital Design principles and practices”, PHI publications, 2005.
4. Mark Zwolinski, “Digital System Design with VHDL” Pearson Education, 2004.
5. H.Charles Roth, “Fundamentals of Logic design”, Thomson Learning, 2003.


**WEB LINKS**

1. http://nptel.ac.in/courses/117106086/
2. http://nptel.ac.in/courses/117108040/
3. http://nptel.ac.in/courses/117105080/

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO2 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO3 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO4 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO5 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL16103** **VLSI DESIGN TECHNIQUES** **3 2 0 4**

**COURSE OBJECTIVES**

- To study the basics of MOS transistor and IC fabrication.
- To learn the characteristics of inverters and logic function.
- To understand the circuit characterization and performance estimation.
- To study VLSI circuits.
- To learn Verilog HDL and design VLSI circuits.

**UNIT I VLSI DESIGN PROCESS AND MOS TRANSISTOR THEORY 15**

VLSI Design Process – Architectural Design – Logical Design – Physical Design – Layout Styles –Full custom, Semicustom approaches.MOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model, Non ideal I-V effects, DC transfer characteristics, VLSI Design flow.

**UNIT II INVERTERS AND LOGIC GATES 15**

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

**UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 15**

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining, Charge sharing, Scaling

**UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS 15**

Multiplexers, Decoders, comparators, priority encoders, Shift registers Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers.

**UNIT V VERILOG HARDWARE LANGUAGE 15**

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Understand basics of MOS transistor and IC fabrication.
- Know inverters characteristics and logic function.
- Estimate the characterization of circuits and its performance.
- Analyze the concepts of VLSI circuits.
- Understand Verilog HDL and design VLSI circuits.

**REFERENCES**


1. Jan M Rabaey, “Digital Integrated Circuits”, Prentice Hall of India, 2002.
2. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits- Analysis and Design”, Tata McGraw Hill, 2003.
3. Neil H.E. Weste and Kamran Eshraghian, “Principles of CMOS VLSI Design”, Pearson Education, ASIA, 2nd edition, 2000.
4. J.Bhasker, B.S.Publications, “A Verilog HDL Primer”, 2nd Edition, 2001.
5. Wayne Wolf “Modern VLSI Design System on chip”, Pearson Education, 2002.


**WEB LINKS**

1. http://nptel.ac.in/courses/117106092/
2. http://nptel.ac.in/courses/Webcourse-contents/IIT Bombay/VLSI%20Design/Course% 20Objective.html
3. http://www.youtube.com/watch?v=9SnR3M3CIm4

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO2 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO3 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO4 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |
| CO5 | 3 | 3 | - | - | 3 | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL16104 SOLID STATE DEVICE MODELING AND SIMULATION 3 2 0 4**

**COURSE OBJECTIVES**

- To know the basic semiconductor physics.
- To understand the basic concepts bipolar device modeling.
- To know the operation of MOSFET modeling.
- To understand the operation parameter measurement.
- To study the characteristics and functions of optoelectronic device modeling.

**UNIT I SEMICONDUCTOR PHYSICS 15**

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources- Diodes : Forward and Reverse biased junctions – Reverse bias breakdown – Transient and AC conditions – Static and Dynamic behavior- Small and Large signal models – SPICE model for a Diode – Temperature and Area effects on Diode Model Parameters.

**UNIT II BIPOLAR DEVICE MODELING 15**

Transistor Models: BJT – Transistor Action – Minority carrier distribution and Terminal currents - Switching- Eber - Molls and Gummel Poon Model, SPICE modeling - temperature and area effects.

**UNIT III MOSFET MODELING 15**

MOS Transistor – NMOS, PMOS – MOS Device equations - Threshold Voltage – Second order effects – Temperature, Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

**UNIT IV PARAMETER MEASUREMENT 15**

Bipolar Junction Transistor Parameter – Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques, Gummel Plots, MOSFET: Long and Short Channel Parameters, Measurement of Capacitance.

**UNIT V OPTOELECTRONIC DEVICE MODELING 15**

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the fundamental of semiconductor physics.
- Understand bjt modeling.
- Understand and design mosfet modeling.
- Analyze optoelectronic device modeling methods.

**REFERENCES**


1. Ben.G.Streetman, “Solid State Devices”, Prentice Hall, 1997.
2. Giuseppe Massobrio and Paolo Antogentti, “Semiconductor Device Modeling with SPICE”, Second Edition, McGraw-Hill Inc, New York, 1993.
3. Mohammed Ismail & Terri Fiez “Analog VLSI-Signal & Information Processing” 1st edition, Tata McGraw Hill Publishing Company Ltd 2001.
4. Roulston E.J., “Bipolar Semiconductor Devices”, Mc-Graw Hill, 1990.
5. Tor.A.Fijedly, “Introduction to Device Modelling and Circuit Simulation”, Wiley-interscience, 1997.


**WEB LINKS**

1. https://www.youtube.com/watch?v=Kp-jS6NHsB8&list=PLF178600D851B098F
2. http://nptel.ac.in/courses/117106091/

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

**PVL16105** **VLSI DESIGN LABORATORY I** **0 0 4 2**

## COURSE OBJECTIVES

- To understand HDL and design circuits using it.
- To gain the ability to write the programs in VHDL and Verilog for modeling digital circuits
- To study and verify the combinational and sequential logic circuits with various levels of modeling and EDA Tools.
- To know importance of basic electronics involved in the design of MOS circuits.

## LIST OF EXPERIMENTS

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using Verilog.
3. Writing Test Benches Using Verilog / VHDL
4. Design and Implementation of ALU using FPGA.
5. Simulation of NMOS and CMOS circuits using SPICE.
6. Design of Static and Dynamic Logic Circuits
7. Modeling of MOSFET using C.
8. Implementation of FFT, Digital Filters.
9. Implementation of DSP algorithms using software package.
10. Implementation of MAC Unit using FPGA.

**TOTAL: 60 PERIODS**

## COURSE OUTCOMES

At the end of this course, the students will be able to

- Make models of transistor circuits and simulate them for various operational requirements.
- Design the different types of multiplier using eda tool.
- Design the fir filter using eda tool.
- Analyze and design the VLSI circuits.

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |

**SEMESTER II**

**PVL16201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 2 0 4**

**COURSE OBJECTIVES**

- To understand the operation of integrated circuits.
- To analyze various devices in circuit configuration of integrated circuit.
- To impart in-depth knowledge about CMOS operational amplifier.
- To explore the concepts of PLL and its application.
- To learn fundamental concepts on ADC and DAC converters.

**UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 15**

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor

**UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 15**

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references - Output stages: Emitter follower, source follower and Push pull output stages.

**UNIT III CMOS OPERATIONAL AMPLIFIERS 15**

Buffered operational amplifiers-High speed and frequency operational amplifiers-Differential output operational amplifiers-Microwave operational amplifiers - Low noise operational amplifiers - Low voltage operational amplifiers

**UNIT IV ANALOG MULTIPLIER AND PLL 15**

Analysis of four quadrant and variable transconductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

**UNIT V DIGITAL-ANALOG AND ANALOG-DIGITAL CONVERTERS 15**

Introduction and characterization of DAC-Parallel DAC-Extending the resolution of parallel DAC-SerialDAC-Introduction and characterization of ADC-Serial ADC-Medium ADC-High speed ADC.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know basic definitions and overview of CMOS integrated circuit.
- Acquire knowledge of how circuit configuration is made for Linear IC.
- Analyze the problems in operational amplifier.

- Understand noise in analog amplifier circuit from a hierarchical viewpoint.
- Apply advanced technical knowledge in MOS technology

**REFERENCES**


1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", 4th Edition, Wiley International, 2002.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", S.Chand and company ltd, 2000
3. Nandita Dasgupata, Amitava Dasgupta, "Semiconductor Devices, Modelling and Technology", Prentice Hall of Indiapvt.ltd, 2004.
4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.


**WEB LINKS**

1. http://nptel.ac.in/courses/117107094/
2. https://www.youtube.com/watch?v=WezDgErVQWU&list=PLC19EACF93A23928B
3. http://nptel.ac.in/courses/117106030/

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16202 COMPUTER AIDED DESIGN OF VLSI CIRCUITS 3 2 0 4**

**COURSE OBJECTIVES**

- To introduce the basic CAD algorithm
- To understand the Partitioning
- To study about placement, floor planning
- To learn about the classification of global routing algorithm
- To know the modeling and synthesis in CAD flow.

**UNIT I LOGIC SYNTHESIS & BASIC ALGORITHMS 15**

Introduction to combinational logic synthesis - Binary Decision Diagram - Hardware models for High-level synthesis - graph algorithms - computational geometry algorithms.

**UNIT II PARTITIONING 15**

Classification of partitioning algorithms - Group migration algorithms - simulated annealing & evolution, other partitioning algorithms

**UNIT III PLACEMENT, FLOOR PLANNING & PIN ASSIGNMENT 15**

Simulation base placement algorithms, other placement algorithms - constraint based floor planning - floor planning algorithms for mixed block & cell design - General & channel pin assignment for register minimization

**UNIT IV ROUTING 15**

Classification of global routing algorithms - Maze routing algorithm - line probe algorithm - Steiner Tree based algorithms - ILP based approaches-classification of routing algorithms - single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

**UNIT V MODELING AND SYNTHESIS 15**

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the fundamentals of basic algorithm in CAD.
- Study the different partitioning algorithm.
- Understand the floor planning and placement algorithm.
- Know the different routing algorithms.
- Know about modeling and synthesis techniques of CAD.

**REFERENCES**


1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das, "Networks-on-Chip "Architectures - A Holistic Design Exploration", Springer.
2. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.
3. Frank Ghenassia, "Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems", Springer © 2005 (281 pages), ISBN: 9780387262321.
4. Luca Benini and Giovanni De Micheli, "Networks on Chips: Technology and Tools", Morgan Kaufmann Publishers © 2006 (408 pages), ISBN: 9780123705211.
5. Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Chips theory and practice", CRC press.


**WEB LINKS**

1. https://www.youtube.com/watch?v=jZ6LAcHmvng
2. www.ece.rice.edu/~kmram/elec523/Notes/general-introduction.pdf
3. http://nptel.ac.in/courses/106105034/

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16203** **VLSI SIGNAL PROCESSING** **3 2 0 4**

**COURSE OBJECTIVES**

- To understand the basic concepts of DSP algorithms.
- To know the concept of retiming folding and unfolding.
- To analyze the various pipelining and parallel processing techniques.
- To study the retiming and unfolding algorithms for various DSP applications.
- To analyze the concept of various filters.

**UNIT I DSP SYSTEMS 15**

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

**UNIT II RETIMING, FOLDING AND UNFOLDING 15**

Retiming - definitions and properties Retiming techniques; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Folding – Folding transformation – Register minimizing techniques – Register minimization in folded architectures.

**UNIT III FAST CONVOLUTION 15**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm –Iterated Convolution – Cyclic Convolution; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

**UNIT IV BIT–LEVEL ARCHITECTURE AND SYSTOLIC ARRAY DESIGN 15**

Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh- Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement. Systolic array design methodology – FIR systolic Arrays – selection of scheduling vector-matrix multiplication and 2D systolic array design-Systolic design for space representations containing Delays

**UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 15**

Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

**TOTAL: 75 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- know DSP algorithms
- understand and analyse the concept of pipelining and other processing for DSP applications
- study about programming of digital signal processors

**REFERENCES**


1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
3. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. Jose E. France and Yannis T sividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
5. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.


**WEB LINKS**

1. http://nptel.ac.in/courses/117102060/
2. https://www.youtube.com/watch?v=dM1y6ZfQkDU&list=PLqZ3SwXz_MlHEYL7xlpsc2x6wfPlyg53
3. http://nptel.ac.in/courses/117101001/

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 |

**PVL16204** **VLSI DESIGN LAB II** **0 0 4 2**

**COURSE OBJECTIVES**

- To implement 8 Bit ALU in FPGA / CPLD
- To implement 4 Bit Sliced processor in FPGA / CPLD
- To implement elevator controller using embedded microcontroller
- To implement alarm clock controller using embedded microcontroller
- To implement model train controller using embedded microcontroller
- To implement the system design using PLL

**LIST OF EXPERIMENTS**

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD
3. Implementation of Elevator controller using embedded microcontroller.
4. Implementation of Alarm clock controller using embedded microcontroller.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.
7. Design and simulation of circuits for gate level event driven simulation.
8. Design and simulation of BIST architectures
9. Design of Minimum Spanning Tree and Partitioning Algorithm.
10. Mini Project

**TOTAL: 60 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Write HDL code for basic as well as advanced digital integrated circuits.
- Import the logic modules into FPGA boards.
- Synthesize place and route the digital ICS.
- Design, Simulate and Extract the layouts of Analog IC Blocks using EDA tools.

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | 3 | 3 |

## ELECTIVE I

**PVL16151 LOW POWER VLSI DESIGN 3 0 0 3**

### COURSE OBJECTIVES

- To know the sources of power consumption in CMOS circuits
- To understand the various power reduction techniques and the power estimation methods.
- To study the design concepts of low power circuits.

### UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

### UNIT II POWER OPTIMIZATION 9

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers CMOS Circuits design styles, Adders, Multipliers

### UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

### UNIT IV POWER ESTIMATION 9

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis- Random Logic signals – Probabilistic power analysis techniques

### UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power –Behavioral level transforms- Software design for low power-– Sources of software power Dissipation – Software Power Estimation –Software Power optimization

**TOTAL: 45 PERIODS**

### COURSE OUTCOMES

At the end of this course, the students will be able to

- Know the basic concepts and principles of CMOS.
- Know the techniques of reducing power consumption
- Understand advanced and special techniques for low power systems
- Analyze the techniques involved in power estimation
- Design the software for low power.

### REFERENCES


1. K.Roy and S.C. Prasad , “Low Power CMOS VLSI circuit design”, Wiley, 2000
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Circuits For Low Power”, Kluwer,2002
3. J.B. Kuo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.

4. A.P.Chandrakasan and R.W. Broadersen, “Low power digital CMOS design”, Kluwer, 1995.
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

**WEB LINKS**

1. https://www.youtube.com/watch?v=ruClwamT-R0&list=PLTEh-62_zAfHmJE-pcjgREKiKyPSgjkxj
2. textofvideo.nptel.iitm.ac.in/106105034/lec1.pdf
3. www.cpdee.ufmg.br/~frank/lectures/Sill-LowPower2.ppt
4. http://nptel.ac.in/courses/106105034/

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

**PVL16152** **ASIC DESIGN** **3 0 0 3**

**COURSE OBJECTIVES**

- To study the design flow and different types of ASIC.
- To familiarize the different types of programming technologies and logic devices.
- To learn the architecture of different types of FPGA.
- To understand the logic synthesis and testing.
- To gain knowledge about partitioning, floor planning, placement and routing.

**UNIT I ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9**

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance-Logicaleffort – Library cell design - Library architecture.

**UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9**

Anti-fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

**UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX – Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

**UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9**

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation

**UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9**

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Understand different types of ASIC’s.
- Know programmable ASIC’s logic cell and I/O cells.
- Study the programmable ASIC interconnect and software.
- Understand logic synthesis and testing.
- Know the concepts of placement and routing.

**REFERENCES**


1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.
3. Wayne Wolf, "FPGA-Based System Design", Prentice Hall PTR, 2004.
4. J.Bhaskar, "A VHDL Synthesis Primer", BS Publications, 2001.
5. J.Bhaskar "VHDL Coding Styles and Methodologies", BS Publications, 2005.


**WEB LINKS**

1. https://www.youtube.com/watch?v=q3po_gNaTBw&list=PLgt7vY9oZ0Wwp53Mrlg_KxQYCMGnebHXR
2. staff.fit.ac.cy/com.tk/ACOE361/Design_Flow.ppt
3. https://www.youtube.com/watch?v=vxSvQ-IcmHM

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

**PVL16153 HARDWARE DESIGN VERIFICATION TECHNIQUES 3 0 0 3**

**COURSE OBJECTIVES**

- To understand the concepts of verification techniques and tools.
- To study the concepts of verification plan, stimulus and response.
- To know the concepts of architecting test benches and system Verilog.

**UNIT I VERIFICATION TECHNIQUES AND TOOLS 9**

Testing vs. Verification – Verification and Design Reuse - Functional Verification, Timing Verification, Formal Verification, Linting Tools – Simulators – Third Party Models – Waveform Viewers – Code Coverage issue – Tracking Metrics

**UNIT II VERIFICATION PLAN 9**

Verification plan – Levels of Verification – Verification Strategies – Specification Features – Test cases – Test Benches

**UNIT III STIMULUS AND RESPONSE 9**

Simple Stimulus – Output Verification – Self Checking Test Benches – Complex Stimulus and Response – Prediction of Output\

**UNIT IV ARCHITECTING TEST BENCHES 9**

Reusable Verification Components – VHDL and Verilog Implementation – Autonomous Generation and Monitoring– Input and Output Paths – Verifying Configurable Design

**UNIT V SYSTEM VERILOG 9**

Data types, RTL design, Interfaces, clocking, Assertion based verification, classes, Test bench automation and constraints.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Use hardware description language to design and simulate a combinational logic circuit.
- Apply hardware description language to describe and simulate sequential designs in more complex systems.
- Understand and apply timing issues in multiple contexts and design the circuit.
- Design digital systems using modern design tools.

**REFERENCES**


1. Janick Bergeron, “Writing Test Benches Functional Verification of HDL Models”, Springer, 2003.
2. Samir Palnitkar, “Design Verification with E”, Prentice Hall, 2003
3. T.Kropf, “Introduction to Formal Hardware Verification”, Springer Verlag, 2010.
4. Chris Spear, “System Verilog for Verification: A Guide to Learning the Test bench Language Features”, Springer, 2008.

5. Janick Bergeron, Edward Cerny, Alan Hunter and Andrew Nightingale, “Verification Methodology Manual for System Verilog”, Springer, 2005.

**WEB LINKS**

1. http://nptel.ac.in/courses/106103016/
2. https://www.youtube.com/watch?v=crBvULemVcQ&list=PL6tk8xkG6ZQc3TNr4D_6WVQOpb1D-IdeW

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

**PVL16154 COMMUNICATION NETWORKS 3 0 0 3**

**COURSE OBJECTIVES**

- To study about the wired and wireless LANs and backbone networks.
- To gain indepth knowledge about the routing protocol and congestion controls.
- To focus on simulation and modeling of qualnet and NS2 simulators.

**UNIT I WIRED LANS 9**

Standard Ethernet- Mac sub layer-physical layer, Bridged Ethernet, switched Ethernet, Fast Ethernet, Gigabit Ethernet. Backbone Networks Connecting devices, Hubs, Bridges, Routers, Gateway, three layer switches, Virtual LAN-SONET**.**

**UNIT II FLOW/CONGESTION CONTROL 9**

Implementation, modeling, fairness, stability, open-loop vs. closed-loop vs. hybrid, traffic specification (LBAP, leaky-bucket), window vs. rate, hop-by-hop vs. end-to-end, implicit vs. explicit feedback, aggregate flow control, reliable multicast TCP variants (Tahoe, Reno, Vegas, New-Reno, SACK), DEC bit, Packet Pair, NETBLT, ATM Forum EERC, T/TCP

**Scheduling and Buffer Management**

Implementation, fairness, performance bounds, admission control, priorities, work conservation, scheduling best effort(BE) flows, scheduling guaranteed-service (GS) flows (GPS, WRR, DRR, WFQ, EDD, RCSP), aggregation, drop strategies (tail-drop, RED, WRED)

**UNIT III ROUTING 9**

Implementation, stability/convergence, link-state vs. distance-vector vs. link-vector, conventional routing, Routing Information Protocol (RIP), Open Shortest Path First (OSPF), Multicast OSPF (MOSPF), Distance Vector Multicast Routing Protocol (DVMRP), BGP instability, Fair queuing, TCP congestion control, TCP variants, Random Early Detect, TCP RTT estimation, Fast retransmit, Fast recovery.

**UNIT IV CONGESTION CONTROL 9**

Congestion Control-open loop-closed loop, congestion control in TCP, congestion control in Frame relay-Quality of service- Integrated Services, Resource Reservation Protocol (RSVP), Differentiated Services, Overlay Networks, Peer-to-Peer Networks, Chord.

**UNIT V SIMULATION AND MODELING 9**

Wide-Area Traffic Modeling, End-to-end Internet Packet Dynamics, Traffic engineering, Multi-Protocol Label Switching (MPLS), Network Simulators- NS2, OPNET, QualNet.

**IP Next Generation**

IP Next Layer (IPNL), IPV6 features, including transition, Mobile IPV6 operation, Models to support (WLAN) network roaming, IPV6 transition methods, Advanced IP routing and multihoming, IP Multicast.

**TOTAL: 45 PERIODS**

## COURSE OUTCOMES

At the end of this course, the students will be able to

- Identify the types of networks and protocols for a given network scenario.
- Estimate the performance and throughput of a given network.
- Design a network aimed at optimum performance.
- Understand the traffic modeling and congestion control in networks.

## REFERENCES


1. Larry Peterson and Bruce Davie, "Computer Networks: A Systems Approach", Morgan Kaufmann, 2007.
2. Michael A Gallo and William M Hancock, "Computer Communications and Networking Technologies", Thomson Learning, 2002.
3. Jim Kurose and Keith Ross, "Computer Networking: A Top-Down Approach Featuring the Internet", Addison- Wesley, 2004.
4. William Stallings, "Data and Computer Communications", Prentice Hall, 2006.
5. Behrouz Forouzan, "Data communications and Networking", TMH, 2007


## WEB LINKS

1. https://www.youtube.com/watch?v=sG6WGvzmVaw&list=PL374944B232C0B48E
2. http://nptel.ac.in/courses/117105076/

## CO-PO Mapping:

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

## ELECTIVE II

**PVL16251 CMOS VLSI DESIGN 3 0 0 3**

**COURSE OBJECTIVES**

- To understand the basic of CMOS circuits.
- To learn the CMOS process technology.
- To study the techniques of chip design using programmable devices.
- To learn the concepts of designing VLSI subsystems.
- To focus on the concepts of modeling a digital system using hardware description language.

**UNIT I MOS TRANSISTOR THEORY 9**

Introduction to I.C Technology- Basic MOS transistors - Threshold Voltage -Body effect - Basic D.C. Equations - Second order effects - MOS models - Small signal A.C characteristics - The complementary CMOS inverter - DC characteristics - Static Load MOS inverters - The differential inverters - Transmission gate.

**UNIT II CMOS PROCESSING TECHNOLOGY 9**

Silicon semiconductor technology - Wafer processing, Oxidation, epitaxy, deposition, Ion implantation - CMOS technology – n-well, p-well process - Silicon on insulator - CMOS process enhancement - Interconnectand circuit elements. Layout design rules - Latchup

**UNIT III CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION 9**

Resistance estimation - Capacitance estimation.MOS capacitor characteristics -Device capacitances - Diffusion capacitance Routing capacitance - Distributed RC effects - Inductance - Switching characteristics Rise time - Fall time. Delay time. Empirical delay models - Gate delays. CMOS gate transistor sizing - Power dissipation. Scaling of MOS transistor dimensions

**UNIT IV CMOS CIRCUIT AND LOGIC DESIGN 9**

CMOS Logic gate design - Fan in and fan out. Typical CMOS NAND and NOR delays - Transistor sizing - CMOS logic structures - Complementary logic - BICMOS logic - Pseudo nMOS logic - Dynamic CMOS logic -Clocked CMOS logic - Pass transistor logic. CMOS domino logic.NP domino logic - Dual rail logic with suitable examples - Cascade voltage switch logic. Source follower pull up Logic (SFPL). Clocking strategies – I/O structures - Comparison of circuit families`

**UNIT V CMOS SUBSYSTEM DESIGN 9**

Data path operations - Addition/subtraction - Parity generators – Comparators - Zero/one detectors - Binary Counters - ALUs, Design of multipliers: Parallel Multipliers, Array, 2's Complement, Booth - Braun – Baugh - Wooley - Wallace tree, Dadda Multipliers, Serial Multiplication – Shifters - Memory elements - RWM, ROM, Content Addressable Memory. Control: FSM, PLA Control Implementation.

**TOTAL: 45 PERIODS**

## COURSE OUTCOMES

At the end of this course, the students will be able to

- Differentiate the ideal and non-ideal characteristics of MOSFET.
- Know various methodologies to fabricate an IC.
- Understand the switching characteristics and power reduction techniques.
- Know the circuit families.
- Design and analyze different CMOS subsystems.

## REFERENCES


1. Neil.H.E. Weste and K.Eshragian, "Principles of CMOS VLSI Design", 2nd Edition. Addison-Wesley, 2000.
2. Douglas a. Pucknell and K.Eshragian., "Basic VLSI Design" 3rd Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., "CMOS Circuit Design", 3rd Indian reprint, PHI, 2000.
4. N.Weste and D.Harris, "Introduction to CMOS VLSI design", Addision- , 3rd Edition, 2004.


## WEB LINKS

1. http://nptel.ac.in/courses/Webcourse-contents/IIT-Bombay/VLSI%20Design/Course%20Objective.htm
2. https://www.youtube.com/watch?v=4It_j_Y944o
3. https://www.youtube.com/watch?v=9SnR3M3CIm4

## CO-PO Mapping:

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16252 DESIGN OF SEMICONDUCTOR MEMORIES 3 0 0 3**

**COURSE OBJECTIVES**

- To acquire basic knowledge about SRAMs and DRAMs
- To study about Non Volatile memories and their types
- To know about fault modeling and testing in memories
- To introduce the concept of reliability and radiation effects in memories
- To gain knowledge in packaging technologies for memories

**UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES 9**

**Static Random Access Memories (SRAMS):**

SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon on Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

**Dynamic Random Access Memories (DRAMs):**

DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

**UNIT II NONVOLATILE MEMORIES 9**

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

**UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AN FAULT TOLERANCE 9**

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

**UNIT IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS 9**

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification- RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

**UNIT V ADVANCED MEMORY TECHNOLOGY 9**

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory Devices -Memory Hybrids

and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

**TOTAL: 45 PERIODS**

## COURSE OUTCOMES

At the end of this course, the students will be able to

- Use the technology behind random access memories
- Understand the nonvolatile memories
- Know about fault modeling and testing of memories
- Know the concepts of memory reliability and packaging technologies

## REFERENCES


1. Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability", Wiley-IEEE Press, 2002.
2. Ashok K. Sharma, "Semiconductor Memories, Two-Volume Set", Wiley-IEEE Press, 2003.
3. Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability", Prentice Hall of India, 1997.
4. Brent Keeth, R. Jacob Baker, "DRAM Circuit Design: A Tutorial", Wiley-IEEE Press, 2000.
5. Betty Prince, "High Performance Memories: New Architecture DRAMs and SRAMs - Evolution and Function", Wiley, 1999.


## WEB LINKS

1. https://www.youtube.com/watch?v=omxQsvenf9o
2. https://www.youtube.com/watch?v=1vMcBQCWRgo
3. vlsi.daiict.ac.in/files/Memories-Daiict.ppt

## CO-PO Mapping:

Mapping of Course Outcomes with Programme Outcomes:
**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

**PVL16253** **VLSI TECHNOLOGY** **3 0 0 3**

**COURSE OBJECTIVES**

- To understand the purification of silicon in different technologies.
- To impart indepth knowledge about photolithography and etching process.
- To acquire knowledge about deposition, diffusion and ion implantation of different layers.
- To know various methodologies to fabricate an IC.
- To understand the different packaging techniques of VLSI devices.

**UNIT I MATERIAL PROPERTIES, CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 9**

Crystal structure- axes & planes, Crystal defects-Point defects & dislocations Crystal growth- Bridgman, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation inducted Defects.

**UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING 9**

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipment's.

**UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATIO ANDMETALLIZATION 9**

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques - Range theory-Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

**UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION 9**

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

**UNIT V PACKAGING OF VLSI DEVICES 9**

Package types – packaging design consideration – VLSI assembly technology – Package fabrication technology.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the various metallization techniques
- Create three-dimensional device structures and devices.
- Know the methodology to fabricate an ic's.

- Understand and design advanced electronics systems (analog and digital systems).
- Conduct experiments, analyze and interpret data.

**REFERENCES**


1. S.M.Sze, “VLSI Technology”, Mc.Graw Hill Second Edition. 1998.
1. Amarmukherjee, “Introduction to NMOS and CMOS VLSI System design”, Prentice Hall India.2000.
2. James D Plummer, Michael D. Deal, Peter B.Griffin, “Silicon VLSI Technology: fundamentals practice and Modeling”, Prentice Hall India.2000.
3. Wai Kai Chen, “VLSI Technology”, CRC press, 2003.


**WEB LINKS**

1. http://nptel.ac.in/courses/117106093/
2. https://www.youtube.com/watch?v=9SnR3M3CIm4&list=PL7F0047F236A6E731
3. https://www.youtube.com/watch?v=_gpEBYUnj6k

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

**PVL16254 PHYSICAL DESIGN OF VLSI CIRCUITS 3 0 0 3**

**COURSE OBJECTIVES**

- To introduce the basic concepts of VLSI technology
- To study the concepts of placement
- To educate about routing
- To learn about issues in circuit layout
- To introduce generation and compaction

**UNIT I VLSI TECHNOLOGY 9**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms.

**UNIT II PLACEMENT USING TOP-DOWN APPROACH 9**

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratio cut- partition with capacity and I/O constraints - Floor planning: Rectangular dual floor planning- hierarchical approach- simulated annealing- Floor plan sizing- Placement: Cost function- force directed method- placement by simulated annealing- partitioning placement

**UNIT III ROUTING USING TOP DOWN APPROACH 9**

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches- hierarchical approaches- multi-commodity flow based techniques-Randomized Routing- One Step approach-Integer Linear Programming Detailed Routing: Channel Routing- Switch box routing.

**UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9**

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Clock Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization.

**UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION 9**

Planar subset problem (PSP) - Single layer global routing- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing- Multiple chip modules (MCM) - Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the basic concepts of VLSI
- Understand the working of placement using top-down approach

- Know about the concepts of routing
- Learn about performance issues in layout
- Know about the generation and compaction of cell

**REFERENCES**


1. Ban Wong, Anurag Mittal, Yu Cao, Greg Starr, "Nano CMOS Circuit and Physical Design", Wiley-IEEE press, 2004.
2. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", Mc Graw Hill International Edition 1995.
3. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.
4. Naveed A. Sherwani, "Algorithm for VLSI Physical Design Automation", 3rd Edition Springer, 1998.
5. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design Automation, Theory and Practice", World Scientific Publishing Company, 1st Edition, 1999.


**WEB LINKS**

1. https://www.youtube.com/watch?v=6M52YKLH7FU
2. http://nptel.ac.in/courses/117106093/
3. https://www.youtube.com/watch?v=lgnJvFNyMfI

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | - | 3 | - | 3 | - | - | - | - | - | - | - | 3 | 3 |

## ELECTIVE III

**PVL16351** **NANO ELECTRONICS** **3 0 0 3**

### COURSE OBJECTIVES

- To acquire knowledge about the fundamentals of quantum mechanics.
- To study about architecture and operations of different Nano structures.
- To comprehend the low dimension, high speed and low power design techniques and methodologies.

### UNIT I TECHNOLOGY AND ANALYSIS 9

Film Deposition Methods – Lithography- Material removing techniques - Etching and Chemical-Mechanical Polishing - Scanning Probe Techniques.

### UNIT II CARBON NANO STRUCTURES 9

Carbon Clusters - Carbon Nano tubes – Fabrication – Electrical, Mechanical and Vibrational Properties – Applications of Carbon Nano tubes.

### UNIT III LOGIC DEVICES 9

Silicon MOSFET's – Novel materials and alternative concepts – Ferroelectric Field Effect Transistors – Super conductor digital electronics – Carbon Nano tubes for data processing.

### UNIT IV RANDOM ACCESS MEMORIES AND MASS STORAGE DEVICES 9

High Permittivity material for DRAM's – Ferro electric Random Access memories – Magneto- resistive RAM- Hard Disk Drives – Magneto Optical Disks – Rewriteable DVDs based on Phase Change Materials – Holographic Data Storage.

### UNIT V DATA TRANSMISSION AND INTERFACES AND DISPLAYS 9

Photonic Networks – Microwave Communication System – Liquid Crystal Displays – Organic Light emitting diodes.

**TOTAL: 45 PERIODS**

### COURSE OUTCOMES

At the end of this course, the students will be able to

- Analyze the different types of nano structures.
- Understand the different nano device fabrication technology.
- Know about characterization techniques.
- Identify new areas of nano device application.

### REFERENCES


1. Rainer Waser, "Nano Electronics and Technology", Wiley VCH, 2003.
2. Charles Poole, "Introduction to Nano Technology", Wiley Inter science, 2003.
3. C.Wasshuber, Simon, "Simulation of Nano Structures Computational Single-Electronics", Springer-Velag, 2001.

4. Rainer Waser, “Nano Electronics and information technology advanced electronic materials and novel devices”, Wiley –VcH Verlag GmBh-KgaH, Germany, 2005.
5. Mark Reed and Takhee Lee, “Molecular Nano Electronics”, American Scientific Publisher, California, 2003.

**WEB LINKS**

1. https://www.youtube.com/watch?v=tW1-fSRiAdc&list=PL7D9EF0D4137E1765
2. web.stevens.edu/.../Nanotechnology/Intro_NANO_Barr_FisherFIN.ppt
3. https://www.youtube.com/watch?v=kCTED1wlQBU

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16352 ADVANCED MICROPROCESSORS AND MICRO CONTROLLERS 3 0 0 3**

**COURSE OBJECTIVES**

- To expose the fundamentals of microprocessor architecture.
- To introduce the advanced features in microprocessors and microcontrollers.
- To enable the students to understand various microcontroller architectures.
- To understand in build function of Controller.

**UNIT I MICROPROCESSOR ARCHITECTURE 9**

Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC – RISC properties – RISC evaluation – On-chip register files versus cache evaluation.

**UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9**

The software model – functional description – CPU pin descriptions – RISC concepts – bus operations – Super scalar architecture – pipe lining – Branch prediction – The instruction and caches – Floating point unit – protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts – Input /Output – Virtual 8086 model – Interrupt processing -Instruction types – Addressing modes – Processor flags – Instruction set -programming the Pentium processor.

**UNIT III HIGH PERFORMANCE RISC ARCHITECTURE: ARM 9**

The ARM architecture-ARM assembly language program-ARM organization and implementation-The ARM instruction set - The thumb instruction set – ARM CPU cores.

**UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS 9**

Instructions and addressing modes – operating modes – Hardware reset – Interrupt system – Parallel I/O ports – Flags – Real time clock – Programmable timer – pulse accumulator – serial communication interface – A/D converter – hardware expansion – Assembly language Programming.

**UNIT V FREE SCALE COLD FIRE 32 BIT PROCESSOR 9**

Introduction to Cold Fire Core, User and Supervisor Programming Model, Addressing modes, Special instructions, Exceptions and Interrupt controller, EMAC, - The MCF5223X Microprocessor- The 5223X Microprocessor, SDRAM controller, Flex CAN, Fast Ethernet Controller, USB.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Design and implement of advanced microprocessor.
- Know about the high performance risc and cisc architecture.
- Perform pic microcontroller programming.
- Know about the various special purpose processors.

**REFERENCES**


1. Daniel Tabak , “Advanced Microprocessors”, McGraw Hill. Inc., 1995
2. Steve Furber, “ARM System –On –Chip architecture”, Addison Wesley, 2000.
3. Gene.H.Miller, “Micro Computer Engineering”, Pearson Education, 2003.
4. Valvano, “Embedded Microcomputer Systems”, Thomson Asia Pvt Ltd first reprint 2001.
5. Munir Bannaoura, Rudan Bettelheim and Richard Soja, “ColdFire Microprocessors and Microcontrollers”, AMT Publishing, 2007


**WEB LINKS**

1. http://nptel.ac.in/courses/106108100/
2. https://www.youtube.com/watch?v=liRPtvj7bFU&list=PL7C177BFA6F3C6544
3. cache.freescale.com/files/32bit/doc/prod_brief/MCF5251PB.pdf

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16353 NEURAL NETWORKS AND APPLICATIONS 3 0 0 3**

**COURSE OBJECTIVES**

- To study the concepts of biological and artificial neurons
- To explore the fundamentals of various algorithms related to supervised neural networks and its applications
- To explore the Applications of various algorithms related Genetic algorithms and SVM

**UNIT I LEARNING ALGORITHMS 9**

Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feed forward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering – Beam forming – Memory – Adaptation - Statistical Learning Theory

**UNIT II RADIAL-BASIS FUNCTION NETWORKS & SUPPORT VECTOR HINES 9**

**Radial Basis Function Networks:**

Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification

**Support Vector Machines:**

Optimal Hyper plane for Linearly Separable Patterns and Non separable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem - -insensitive Loss Function – Support Vector Machines for Nonlinear Regression

**UNIT III ATTRACTOR NEURAL NETWORKS 9**

Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications.

**UNIT IV ADAPTIVE RESONANCE THEORY 9**

Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center –Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of ResonanceModel – Adaptive Resonance Theory – Applications.

**UNIT V SELF ORGANIZING MAPS AND NEOCOGNITRON 9**

Self-organizing Map – Maximal Eigenvector Filtering – Sanger's Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications. Architecture of Neocognitron – Data processing and performance of Neocognitron - Architecture of spatio – temporal networks for speech recognition.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Understand the basics of neural networks.
- Know the concepts of radial basis functions.
- Gain knowledge about bidirectional associative memory.
- Understand the principles of resonance theory.
- Know the self-organizing maps.

**REFERENCES**


1. Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.
2. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.
3. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques", Pearson Education 2003.
4. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2nd Edition, Prentice Hall India, 2002.
5. Martin T.Hagan, Howard B. Demuth, and Mark Beale, "Neural Network Design", Thomson Learning, New Delhi, 2003.


**WEB LINKS**

1. https://www.youtube.com/watch?v=xbYgKoG4x2g
2. http://nptel.ac.in/courses/117105084/
3. www.cse.iitd.ac.in/~saroj/AI/ai2013/L22.ppt

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | 3 | | | | | | | | | | | 3 | 3 |

**PVL16354 RELIABILITY ENGINEERING 3 0 0 3**

**COURSE OBJECTIVES**

- To introduce the basics of probability
- To understand the concepts of reliability
- To educate about software system reliability
- To learn about testing
- To introduce reliability management

**UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9**

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

**UNIT II RELIABILITY PREDICTION, MODELING AND DESIGN 9**

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte Carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

**UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9**

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces

**UNIT IV RELIABILITY TESTING AND ANALYSIS 9**

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring

**UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT 9**

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Understand the basic probability concepts and interference.
- Incorporate the concepts of modeling and design.
- Know about testing and analysis.
- Understand manufacture and reliability management.

**REFERENCES**


1. Patrick D.T. O'Connor, David Newton and Richard Bromley, "Engineering, Practical Reliability", Fourth edition, John Wiley & Sons, 2002.
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3. K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.
4. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.


**WEB LINKS**

1. https://www.youtube.com/watch?v=1oNIgAT5nK4&list=PL5089B78A04064D5B
2. https://www.youtube.com/watch?v=zbDRH2ASyqQ
3. asqbaltimore.org/dt/present/Present200401_CusumBasics.ppt

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |

## ELECTIVE IV

**PVL16451 ANALOG VLSI DESIGN 3 0 0 3**

**COURSE OBJECTIVES**

- To acquire basic knowledge about CMOS circuit techniques and amplifier design
- To study about BICMOS circuits and signal processing
- To understand the concepts behind A/D Converters and analog sensors
- To introduce the concept of testing of Analog VLSI circuits
- To gain knowledge about statistical modeling and simulation of analog circuits

**UNIT I CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING 9**

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

**UNIT II BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9**

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models- Design Methodology-Networks-Contrast Sensitive Silicon Retina.

**UNIT III ANALOG CMOS SUB CIRCUITS 9**

CMOS Amplifiers MOS switch-MOS diode and active resistor-Current sinks and sources-Current mirrors-Current and voltage References:-Band gap References:-Invertors-Differential amplifiers - Cascode amplifiers – Current amplifiers - Output amplifiers- High gain amplifiers architectures

**UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9**

Fault modeling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines- Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses- Design for Electron -Beam Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

**UNIT V DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS 9**

Introduction and characterization of DAC-Parallel DAC-Extending the resolution of parallel DAC-Serial DAC- Introduction and characterization of ADC-Serial ADC-Medium ADC-High speed ADC.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the CMOS circuit design and low voltage signal processing

- Understand the basic BI-CMOS circuit techniques and models.
- Know about sampled data analog filters and A/D Converters
- Perform the statistical modeling and simulate the analog circuits

**REFERENCES**


1. Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing", McGraw- Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, "Analog VLSI Design - NMOS and CMOS", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, Noel K.Strader, "VLSI Design Techniques for Analog and Digital Circuits", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing", Prentice Hall, 1994.


**WEB LINKS**

1. https://www.youtube.com/watch?v=dKNzHqLEtYM&list=PL697654290C3A3A1C
2. https://www.youtube.com/watch?v=WDo58OseTJw
3. uhaweb.hartford.edu/ilumokanw/Intro567.ppt

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16452 THREE DIMENSIONAL NETWORKS ON CHIP 3 0 0 3**

**COURSE OBJECTIVES**

- To understand the fundamentals of 3D NOC.
- To impart knowledge about testing and energy issues in NOC.
- To know the concepts of micro-architecture of NOC router.
- To understand the router architectures in 3D NOC.

**UNIT I THREE DIMENSIONAL NOC 9**

Three-Dimensional Networks-on-Chips Architectures – Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on-Chip

**UNIT II TEST AND FAULT TOLERANCE OF NOC 9**

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures- Monitoring Services for Networks-on-Chips

**UNIT III ENERGY AND POWER ISSUES OF NOC 9**

Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: A Complete Industrial Design Flow for Networks-on-Chips

**UNIT IV MICRO-ARCHITECTURE OF NOC ROUTER 9**

Baseline NoC Architecture – MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers- RoCo: The Row-Column Decoupled Router – A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks - Exploring Fault Tolerant Networks- on-Chip Architectures.

**UNIT V DIMDE ROUTER FOR 3D NOC 9**

A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures-Digest of Additional NoC MACRO-Architectural Research

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the 3D NOC and fault tolerance of NOC
- Acquire knowledge, how to analyze the energy and power issues of NOC
- Know the concepts of micro-architecture of NOC router.
- Analyze the problem in DIMDE router.

**REFERENCES**


1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das, “Networks-on-Chip Architectures A Holistic Design Exploration”, Springer, 2009.
2. Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi, “Networks-on-Chips theory and practice”, CRC press, 2009.

3. Axel Jantsch, Hannu Tenhunen, “Networks on Chip”, Publisher: Springer; Soft cover reprint of hardcover 1st ed. 2003 edition (November 5, 2010).
4. Giovanni De Micheli, Luca Benini, “Networks on Chips: Technology and Tools (Systems on Silicon)”, Publisher: Morgan Kaufmann; 1 edition (August 3, 2006).
5. Jose Flich, Davide Bertozzi, “Designing Network On-Chip Architectures in the Nanoscale Era”, (Chapman & Hall/CRC Computational Science), Publisher: Chapman and Hall/CRC; 1 edition (December 18, 2010).

**WEB LINKS**

1. http://nptel.ac.in/courses/117106116/
2. www.eecs.wsu.edu/~pande/Journal_Papers/NoC_3D.pdf
3. www.ece.rochester.edu/users/friedman/papers/TVLSI07_3dnoc.pdf

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL16453 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN 3 0 0 3**

**COURSE OBJECTIVES**

- To understand the basics of EMI & EMC Environment
- To know about EMI & EMC Coupling Principles
- To study the control techniques involved in Electromagnetic Interference
- To learn about EMI Specification Standards and Limits
- To know the concepts of EMI used in instrumentation system

**UNIT I EMI/EMC CONCEPTS 9**

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards

**UNIT II EMI COUPLING PRINCIPLES 9**

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk; Field to cable coupling ; Power mains and Power supply coupling.

**UNIT III EMI CONTROL TECHNIQUES 9**

Shielding- Shielding Material-Shielding integrity at discontinuities, Filtering- Characteristics of Filters-Impedance and Lumped element filters-Telephone line filter, Power line filter design, Filter installation and Evaluation, Grounding- Measurement of Ground resistance-system grounding for EMI/EMC Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control. EMI gaskets

**UNIT IV EMC DESIGN OF PCBS 9**

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits, Component selection and mounting; PCB trace impedance; Routing; Cross talk control-Electromagnetic Pulse-Noise from relays and switches, Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

**UNIT V EMI MEASUREMENTS AND STANDARDS 9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx/Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Frequency assignment – spectrum conversation - British VDE standards, Euro norms standards in Japan –comparisons - EN Emission and Susceptibility standards and Specifications

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Know the concepts of EMI & EMC
- Find solution to EMI sources

- Find solution to EMI problems in PCB level
- Measure emission immunity level from different systems to couple with different standards
- Test and implement EMI system

**REFERENCES**


1. V.P. Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork,2001
2. Henry W.Ott., "Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 2008.
3. Clayton R.Paul, "Introduction to Electromagnetic Compatibility", John Wiley Publications, 2008
4. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC", Vol I-V, 1988.
5. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artechhouse, Norwood, 1987.


**WEB LINKS**

1. https://www.youtube.com/watch?v=4hTOGc93ZTc
2. www.irpel.org/pdf.../electromagnetic-interference-and-compatibility.pdf
3. http://nptel.ac.in/courses/108106073/

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | - | - | - | - | - | - | - | - | - | - | 3 | 3 |
| CO5 | 3 | 3 | | | | | | | | | | | 3 | 3 |

**PVL16454 VLSI FOR WIRELESS COMMUNICATION 3 0 0 3**

**COURSE OBJECTIVES**

- To understand the basics of wireless communication.
- To understand the concepts of transceiver architectures.
- To introduce to the students the low power design techniques of VLSI circuits.
- To learn the design and implementation of various VLSI circuits for wireless communication systems.

**UNIT I WIRELESS COMMUNICATION 9**

Digital communication systems- minimum bandwidth requirement, the Shanon limit- overview of modulation schemes- classical channel- wireless channel description- path loss- multipath fading- basics of spread spectrum and spread spectrum techniques- PN sequence.

**UNIT II TRANSCEIVER ARCHITECTURE 9**

Transceiver design constraints- baseband subsystem design- RF subsystem design- Super heterodyne receiver and direct conversion receiver- Receiver front-end- filter design- non-idealities and design parameters- derivation of noise figure and IP3 of receiver front end.

**UNIT III LOW POWER DESIGN TECHNIQUES 9**

Source of power dissipation- estimation of power dissipation- reducing power dissipation at device and circuit levels- low voltage and low power operation- reducing power dissipation at architecture and algorithm levels.

**UNIT IV WIRELESS CIRCUITS 9**

VLSI Design of LNA-wideband and narrow band-impedance matching - Automatic Gain Control (AGC) amplifier power amplifier- Active mixer- analysis, conversion gain, distortion analysis- low frequency and high frequency case, noise - Passive mixer- sampling mixer and switching mixer- analysis of distortion, conversion gain and noise in these mixers

**UNIT V VLSI DESIGN OF SYNTHESIZERS 9**

VLSI design of Frequency Synthesizers (FS) – Parameters of FS - PLL based frequency synthesizer, phase detector/charge pump- dividers- VCO- LC oscillators- ring oscillator- phase noise- loop filter-description, design approaches.

**TOTAL: 45 PERIODS**

**COURSE OUTCOMES**

At the end of this course, the students will be able to

- Understand the application of VLSI circuits in wireless communication.
- Gain knowledge in the various architectures used in implementing wireless systems.
- Know about design and simulation of low power techniques using software
- Understand the VLSI design of wireless circuits.

**REFERENCES**


1. Bosco Leung, “VLSI for Wireless Communication”, Springer, 2011.
2. Elmad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI Wireless Design-Circuits and Systems”, Kluwer Academic Publishers, 2002.


**WEB LINKS**

1. http://nptel.ac.in/courses/117102062/
2. https://www.youtube.com/watch?v=CUyF0YGIA5Y&list=PL1A4AFAC7AC1909C9
3. www.ccs.neu.edu/home/rraj/Courses/G250/S05/.../SpreadSpectrum.ppt

**CO-PO Mapping:**

| Mapping of Course Outcomes with Programme Outcomes: **(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Programme Outcomes(POs)** | | | | | | | | | | | | | | |
| **CO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** |
| CO1 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 |

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO5** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15301** **TESTING OF VLSI CIRCUITS** **3 2 0 4**

**COURSE OBJECTIVES**

To enable the students to

- gain knowledge on digital testing as applied to VLSI design.
- acquire knowledge on testing of algorithms for digital circuits
- learn various testing methods for digital circuits
- build memory testing
- classify different level of diagnosis

**UNIT I BASICS OF TESTING AND FAULT MODELING** **15**

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

**UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS** **15**

Test generation for combinational logic circuits - Testable combinational logic circuit design - Testgeneration for sequential circuits - design of testable sequential circuits.

**UNIT III DESIGN FOR TESTABILITY** **15**

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - Systemlevel DFT approaches.

**UNIT IV BIST MEMORY TESTING** **15**

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - TestableMemory Design - Test algorithms.

**UNIT V LOGIC LEVEL AND SYSTEM LEVEL DIAGNOSIS** **15**

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

**TOTAL PERIODS** **75**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- observe basics of testing and fault modeling.
- classify different testing algorithms.
- build design for testability.
- practice the concepts of bist and memory testing.
- discriminate different level of fault diagnosis.

**TEXT BOOKS**


1. M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems a Testable Design", Jaico Publishing House, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

3. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers, 2002.
4. A.L. Crouch, “Design for Test for Digital IC's and Embedded Core Systems”, Prentice Hall International, 2002.

Mapping of Course Outcomes with Programme Outcomes:

**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO5** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15551 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- memorize the architecture and various addressing modes of processor.
- impart knowledge on the operation of ADSP and Analog Processors.
- estimate the architectures
- appraise the various addressing modes of TMS320C54X and TMS320C6Xprocessor.

**UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPS** **9**

Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

**UNIT II TMS320C3X PROCESSOR** **9**

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design.

**UNIT III ADSP PROCESSORS** **9**

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors - Addressing modes –and assembly language instructions – Application programs –Filter design, FFT calculation.

**UNIT IV ADVANCED PROCESSORS** **9**

Architecture of TMS320C54X: Pipe line operation, Addressing modes and assembly language instructions Introduction to Code Composer studio.

**UNIT V ADVANCED PROCESSORS II** **9**

Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

**TOTAL PERIODS 45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- analyze the procedure for various DSP system architecture
- diagnose the design methodologies in hardware and software
- perform the identification of new developments in DSP systems.
- design and implement various signal processing techniques using DSP processors.

**TEXT BOOKS**


1. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming andApplications”, Tata McGraw Hill Publishing Company Limited. New Delhi, 2003.
2. User guide, Texas Instrumentation, Analog Devices, Motorola
3. Steven smith, “The scientist and engineers guide to digital signal processing”.
4. Yu Hen Hu, “Programmable digital signal processors: Architecture, Programming andapplication”, CRC press, 2001

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PS O1** | **PS O2** |
| **CO1** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15552 DATA CONVERTERS** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- understand the basic concepts Data converters performances
- work through the A/D converters
- analyze the hardware Design Techniques
- study the concepts of digital correction & calibration
- focus on the application of converters

**UNIT I DATA CONVERSION FUNDAMENTAL, DATA CONVERTER RFORMANCES** **9**

Sampling of Analog Signals - Quantization Error and Quantization Noise -Nyquist Rate and Oversampling – Conversion - Resolution and SNR- Reconstruction-Static Performances -Dynamic Performances – Distortion.

**UNIT II SAMPLE & HOLD CIRCUITS, LOW SPEED NYQUIST-RATE A/D CONVERTERS** **9**

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture. CMOS Track and Sample and Hold-Diode Bridge T&H-Switched Emitter T&H-Accuracy and Speed-Integrating Converter-Successive Approximation Converters-Algorithmic A/D Converters.

**UNIT III HIGH SPEED NYQUIST-RATE A/D CONVERTERS, OVERSAMPLING A/DCONVERTERS** **9**

Flash Converters-Two-Step Converters-Folding Converters-Interpolating Technique-Interleaved Converters-Pipeline Converters-Noise Shaping-First-Order Sigma-Delta - Second-Order Sigma-Delta - High-Order Sigma-Delta-Multi-bit Oversampling Converters-Practical Limit-Design Considerations

**UNIT IV DIGITAL CORRECTION AND CALIBRATION, NYQUIST-RATE DACS** **9**

Digital - Correction-Linearization of Transfer Characteristics - Basic considerations – Switched Capacitor MDAC - Resistive based Architectures - Current Steering D/A Converters.

**UNIT V PRECISION TECHNIQUES** **9**

Comparator offset cancellation - Op Amp offset cancellation - Calibration techniques - range overlap and digital correction.

**TOTAL PERIODS 45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- acquire knowledge of fundamentals of data converters
- learn to analyze the circuit.
- relate a/d & d/a converters
- describe the data converters for various applications

**REFERENCES**


1. D.A. Johns and K. Martin, “Analog Integrated Circuits and Systems”, McGraw-Hill, NY 1994
2. Rudy J, Van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters”, BS Publications, 2005.
3. B. Razavi, “Principles of Data Conversion System Design”, The IEEE Press, New York, 1995.
4. Walt Kester Editor, “Analog-Digital Conversion”, analog devices, 2004
5. Allen Holberg, “CMOS Analog Circuit Design”, PHI
6. Franco Maloberti, “Data Converters”, Springer, 2007.


Mapping of Course Outcomes with Programme Outcomes:

**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| **CO2** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| **CO3** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |
| **CO4** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | - | 3 | 3 |

**PVL15553 ADVANCED EMBEDDED SYSTEMS** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- study the overview of Architecture of Embedded System
- focus on processors used in Embedded Systems
- compare the various networks of Embedded System
- analyses Real Time Systems
- evaluate system design methodologies

**UNIT I EMBEDDED ARCHITECTURE** **9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded System Design, Embedded System Design Process - Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration.

**UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM** **9**

ARM processor- Processor and memory organization, Data operations, Flow of control, SHARC processor- Memory organization, Data operations, Flow of control, Parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory Devices, Input and Output Devices. Design Example: Alarm Clock.

**UNIT III NETWORKS** **9**

Distributed Embedded Architecture - Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link ports, Ethernet, Myrinet, Internet. Network based design, Design Example: Elevator Controller

**UNIT IV REAL-TIME CHARACTERISTICS** **9**

Clock driven Approach, Weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, Off-line Versus On-line scheduling

**UNIT V SYSTEM DESIGN TECHNIQUES** **9**

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX-Ink jet printer- Personal Digital Assistants, Set-topBoxes

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- know about the architecture of embedded system
- design embedded processor architecture.
- know about various networks of embedded system
- understand about real time systems
- demonstrate the basic difference between RTES and RTOS in system design

**TEXT BOOKS**

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”,Morgan

Kaufman Publishers, 2001.

2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia, 2000
3. C. M. Krishna and K. G. Shin , “Real-Time Systems”, McGraw-Hill, 1997
4. Frank Vahid and Tony Givargi, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2000.
5. Rajkamal, “Embedded Systems Architecture, Programming and Design”, TMH, First reprint,2003.

Mapping of Course Outcomes with Programme Outcomes:

**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO5** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15554 ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- understand the MOS transistor circuit and its enhancement process.
- acquire knowledge in generation of MOS inverter circuit for combinational and sequentialcircuits
- understand the concepts behind the high speed logic design
- study the concept of semiconductor memory design
- learn about Power distribution design-clocking and timing issues

**UNIT I DEEP SUBMICRON DIGITAL IC DESIGN, TRANSISTORS AND DEVICES-MOS AND BIPOLAR, FABRICATION, LAYOUT AND SIMULATION** **9**

Review of Digital Logic Gate Design-digital IC design-computer Aided Design of digital circuits-The MOS Transistor-Bipolar Transistor and circuits-IC Fabrication technology-Layout basics-modeling the MOS transistor for circuit simulation-SPICE MOS level1 device model-BSIM3 model-additional effects in MOS transistors-SOI technology.

**UNIT II MOS INVERTERS CIRCUITS, STATIC MOS GATE CIRCUITS** **9**

Voltage transfer characteristics-noise margin definitions-resistive load inverter design-NMOS transistors as load devices-CMOS inverter-pseudo-NMOS inverters-sizing inverters- tristate inverters-CMOS gate circuits-complex CMOS gates-XOR and XNOR gates-multiplexer circuits – Flip-flops and latches – D flip-flops and latches – power dissipation in CMOS gates-power and delay trade-offs.

**UNIT III HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE AND DYNAMIC LOGIC DESIGN** **9**

Switching time analysis – detailed load capacitance calculation – improving delay calculation with input slope - gate sizing for optimal path delay – optimizing path with logical effort – basic concepts of transfer gate – CMOS transmission gate logic – dynamic D latches and D flip-flops – domino logic –voltage bootstrapping.

**UNIT IV SEMICONDUCTOR MEMORY DESIGN, ADDITIONAL TOPICS IN MEMORYDESIGN, INTERCONNECT DESIGN** **9**

Introduction-MOS decoders – static RAM cell design - SRAM column I/O circuitry – memory architecture - content addressable memories - FPGA-dynamic Read - Write memories - Read Only memories-EPROMs and $E^2$PROMs - flash memory – FRAMs - interconnect RC delays - buffer insertion for very long wires - interconnect coupling capacitance - interconnect inductance - antenna effects.

**UNIT V POWER GRID AND CLOCK DESIGN, LOW POWER CMOS LOGIC CIRCUITS, HIP INPUT & OUTPUT CIRCUITS, DESIGN FO TESTABILITY** **9**

Power distribution design-clocking and timing issues, phase-locked loops/delay-locked loops – low power design through voltage scaling – estimation and optimization of switching activity – reduction of switched capacitance – adiabatic logic circuits – ESD protection – input circuits – output circuits and L(di/dt) noise – on-

chip clock generation and distribution – latch-ups and its prevention – fault types and models – controllability and observability – adhoc testable design techniques – scan based techniques – Built-In-Self Test(BIST) techniques – current monitoring $I_{DDQ}$ test.

**TOTAL PERIODS 45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- know about importance of logical design vlsi circuits.
- model different faults and carry out fault simulation in digital circuits.
- analyse high speed CMOS circuit
- focus memory device

**TEXT BOOKS**


1. David A Hodges, Horace G Jackson, Resve A Saleh, "Analysis and design of Digital IntegratedCircuits – in deep submicron technology", Tata McGraw Hill, Edition 2005.
2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits-analysis and design", TataMcGraw Hill, Third edition-2003


Mapping of Course Outcomes with Programme Outcomes:

**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| COs | Programme Outcomes(POs) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 |
| CO1 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO2 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO3 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| CO4 | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15651 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- study the fundamentals of parallel processing.
- estimate architecture of processor and memory organization.
- impart knowledge on the operation of pipeline architecture
- illustrate the architecture of vector processing and multithreading.

**UNIT I PRINCIPLES OF PARALLEL PROCESSING** **9**

Multiprocessors and Multicomputers – Multivector and SIMD Computers- PRAM and VLSI Models- Conditions of Parallelism- Program Partitioning and scheduling-program flow mechanisms- parallel processing applications- speed up performance law.

**UNIT II PROCESSOR AND MEMORY ORGANIZATION** **9**

Advanced processor technology – superscalar and vector processors- memory hierarchy technology- virtual memory technology- Cache memory organization- Shared memory organization.

**UNIT III PIPELINE AND PARALLEL ARCHITECTURE** **9**

Linear pipeline processors- Non linear pipeline processors- Instruction pipeline design- Arithmetic design- Superscalar and super pipeline design- Multiprocessor system interconnects- Message passing mechanisms.

**UNIT IV VECTOR, MULTITHREAD AND DATAFLOW ARCHITECTURE** **9**

Vector Processing principle- Multivector Multiprocessors- Compound Vector processing- Principles of multithreading-fine grain multicomputers- scalable and multithread architectures – Dataflow and hybrid architectures.

**UNIT V SOFTWARE AND PARALLEL PROCESSING** **9**

Parallel programming models- parallel languages and compilers- parallel programming environments- synchronization and multiprocessing modes- message passing program development- mapping programs onto multicomputers- multiprocessor UNIX design goals- MACH/OS kernel architecture- OSF/1 architecture and applications.

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- analyze the procedure for various dsp system architecture
- diagnose the design methodologies in hardware and software
- perform identification of new developments in dsp systems.
- design and implement various signal processing techniques using dsp processors.

**REFERENCES**


1. Kai Hwang, “Advanced Computer Architecture”, TMH 2001.
2. William Stallings, “Computer Organization and Architecture”, McMillan Publishing Company.
3. M.J. Quinn, “Designing efficient Algorithms for parallel computer”, McGraw Hill International

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | 3 | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15652 RF IC DESIGN** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- understand the basics of RFICs.
- analyze the RF components and Modeling.
- introduce to the students the basics of Impedance matching in RFICs
- inspect design of active circuits in RFICs
- develop the RF Oscillators and Mixers

**UNIT I INTRODUCTION** **9**

Importance of RF design, dimensions and units, RF Behavior of passive components, chip components and circuit board considerations, RF circuit manufacturing processes , introduction to random process and noises, review of thermal noise, noise models and circuit noise calculations.

**UNIT II ACTIVE RF COMPONENTS AND MODELING** **9**

Semiconductor basics, RF Diode, bi-polar Junction Transistor, RF Field Effect Transistors, Metal Oxide Semiconductor Transistors, High electron mobility transistors, diode and transistor models, Measurement of active devices.

**UNIT III MATCHING-BIASING NETWORK AND RF TRANSISTOR AMPLIFIERDESIGN** **9**

Impedance Matching using Discrete Components, Micro-strip line Matching Networks, Amplifier classes of operations and biasing networks, Amplifier power relations, Stability considerations, Constant gain, Noise Figure circles, constant VSWR Circles, Broad band High power and multistage amplifiers.

**UNIT IV MODULATORS AND DEMODULATORS TECHNIQUES, RF TRANSCEIVERSARCHITECTURES** **9**

Modulators and demodulators, their structures and electrical schemes, transceivers and architectures, Transceivers functions and their characteristics, direct conversions and super heterodyne receivers.

**UNIT V RF OSCILLATORS, MIXERS AND PHASE LOCKED LOOPS (PLL)** **9**

Basic Oscillator models, High-Frequency Oscillator Configuration, Basic characteristics of Mixers-Single ended, double ended, integrated active, and image reject mixers, Phase locked loops and frequency synthesis, Basic building block of the PLL, PLL synthesizers for radio applications

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- classify the various applications of RF IC’s
- gain knowledge of various technologies and parameters.
- discuss about impedance matching and their design and simulation using software
- discriminate the applications of passive circuits and active circuits in RF ICs.

**REFERENCES**


1. Reinhold Ludwig and Gene Bogdanov, "RF Circuit Design", second edition, Pearson Education,2009.
2. D. M. Pozar, "Microwave engineering", second edition, N.Y., John Wiley and Sons, 1998
3. B.P.Lathi, "Modern digital and analog communication systems", third edition, N.Y., OxfordUniversity press, 1998
4. B.Sklar, "Digital communications-fundamentals and applications", second edition, Prentice Hall PTR,New Jersey, 2001.


Mapping of Course Outcomes with Programme Outcomes:

**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak**

| **COs** | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15653 RF MEMS** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- understand the basic concepts of RF MEMS
- acquire the basic knowledge of Micro machined Components I
- know about the Micro machined Components II
- understand the key concepts of beam structures and micro strip antennas
- know the design analysis using RF MEMS

**UNIT I INTRODUCTION & SWITCHING** **9**

Overview of RF MEMS, Road map, fabrication process design and testing, Applications, RF MEMS relays and switches: Switch parameters, Actuation mechanisms, Bistable relays and micro actuators, Dynamics of switching operation.

**UNIT II MICRO MACHINED INDUCTORS AND CAPACITORS** **9**

MEMS inductors and capacitors: Micro machined inductor, Effect of inductor layout, Modeling and design issues of planar inductor, Gap tuning and area tuning capacitors, Dielectric tunable capacitors.

**UNIT III RF MEMS PHASE SHIFTERS** **9**

MEMS phase shifters: Types. Limitations - Switched delay lines, Micro machined transmission lines, coplanar lines, Micro machined directional coupler and mixer.

**UNIT IV MICRO MACHINED FILTERS &ANTENNAS** **9**

Micro machined RF filters: Modeling of mechanical filters, Electrostatic comb drive, Micromechanical filters using comb drives, Electrostatic coupled beam structures. Micro machined antennas: Micro strip antennas – design parameters, Micromachining to improve performance, Reconfigurable antennas.

**UNIT V RF MEMS DESIGN ANALYSIS** **9**

MEMS Physical Modeling, Physical and practical aspects of RF circuit design: X –Band RF MEMS Phase shifter for radar system applications, FBAR filter for PCS applications, A Ka-Band millimeter- wave tunable filter. Impedance mismatch effects in RF MEMS, RF/Microwave substrate properties, MEMS-Resonators.

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- acquire the basic knowledge of rf mems and switching
- gain in-depth knowledge about tuning elements
- demonstrate critical thinking and problem solving capabilities.
- identify the major rf filters and antennas
- design and analyze circuits using rf mems

**REFERENCES**


1. V.K.Varadan, KJ.Vinoy,K.N.Jose, “RFMEMS and their Applications”, Wiley, 2003
2. H.J.Delos Santos, “RF MEMS circuit Design for Wireless Communications”, Artech House, 2002.

3. Gabriel.M.Rebeiz, “RF MEMS Theory, Design and Technology”, John Wiley, 2003

| Mapping of Course Outcomes with Programme Outcomes:<br>**(1/2/3 indicates strength of correlation) 3-Strong, 2-Medium , 1-Weak** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **COs** | **Programme Outcomes(POs)** | | | | | | | | | | | | | |
| | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **CO1** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO2** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO3** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO4** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |
| **CO5** | 3 | 3 | 3 | - | - | - | - | - | - | - | - | 3 | 3 | 3 |

**PVL15654 RECONFIGURABLE COMPUTING** **3 0 0 3**

**COURSE OBJECTIVES**

To enable the students to

- familiarize the PLD devices.
- understand the concepts of reconfigurable architectures.
- study the concepts & gain knowledge about operating systems.
- study mapping and placement
- understand the application of FPGA

**UNIT I DEVICE ARCHITECTURE** **9**

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices –Complex - Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

**UNIT II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS** **9**

Reconfigurable processing fabric architectures – RPF integration into traditional computing systems – reconfigurable computing systems – case studies – reconfiguration management.

**UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS** **9**

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing –operating System Support for Reconfigurable Computing.

**UNIT IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS** **9**

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bit streamGeneration – Case Studies with Appropriate Tools.

**UNIT V APPLICATION DEVELOPMENT WITH FPGAS** **9**

Case Studies of FPGA Applications – System on a programmable Chip (SoPC) Designs.

**TOTAL PERIODS** **45**

**COURSE OUTCOMES**

At the end of the course, the students will be able to

- understand PLD devices.
- analyses the concepts of reconfigurable architectures.
- explain about operating systems
- develop mapping and placement
- design the application of FPGA.

**REFERENCES**


1. Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computationwith Field Programmable Gate Arrays”, Springer, 2005
2. Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing – The Theory and Practice ofFPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, “Introduction to Reconfigurable Computing – Architectures, Algorithms andApplications”, Springer, 2010.